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Research Article

Random Testing of 3-cell NPSF in memories usingLFSR and NLFSR

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Abstract

This paper proposes a new check analysis method for testing of NPSF defects in wide range access memories. LFSR and NLFSR's are used asaddress generators to select a particular cell in thememory. Single bit change sequences are used as a testpatterns to find the active faults. It has one fault cell and two forced unit. It is used to perceive the ANPSF impact on base cell by way of switching of patterns in the corresponding deleted neighborhood cells. The whole ANPSF ideal structure for memory testing is advanced the use of Verilog HDL. The random testing method gives the better performance than the conventional methods. The testing method is implemented using Vivado 14.7 and Nexys four DDR Artix 7 FPGAboard.

Keywords: Active Neighborhood Pattern Sensitive Fault (ANPSF), Three cell neighborhood, Hamiltonian and Gray pattern generator, Vivado 14.7, Nexys Artix Seven.

I. INTRODUCTION

Fast enlarge of closeness inside the built-in circuits has an immediate impact on memory. On other hand, the capability of arbitrary-access memory chips rise, for that reason enhances the test process and cost; on the opposite hand, closeness of memory laps grows, consequently extra failure modes and faults acquired be seized under consideration so as to get a sincere best product. [1] Accordingly, there are two conflicting constraints that require to be addressed when taking a test algorithm, lowering quantity of memory operations so as to permit wide capacity memories to be examined The block subsists of a base cell along with consequently the excluded block, the bottom unit is that the unit underneath test. The neighborhood with the bottom cell excluded is named the excluded block. NPSFs are frequently viewed with reference to all eight excluded neighborhood cells [3]. The proposed approach compresses the overall setup constraint when in variation withthe traditional method and the ANPSF structure is passed down to identify the inaccurate pattern according to the excluded locale cells. This journal is inventoried as follows. phase II explains about the faults, LFSR and NLFSR shift registers. Phase III proposed methodology for ANPSF testing. Section IV illustrates the stimulation results and forming report with the FPGAimplementation on Nexys Artix 7. Section V about the conclusion.

II. PATTERN SENSITIVE FAULTMODEL

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A pattern Sensitive fault may take place when the value of cell or the ability to change the value is influenced by the value of other cells in the memory.[4] The NPSF consists of a base cell and the deleted neighborhood. The base cell is the cell under test. The neighborhood with the base cellexcluded is called the deleted neighborhood. The NPSFs are of three types.[4]

Types of NPSF

Types of NPSFs are classified based on the transitions of base cell and deleted neighborhood cells.

Passive NPSF: The base cell failed to change its value by the influence of neighborhood cells.[5]

Static NPSF: The neighborhood cells forced to change the value of the base cell.[5]Active NPSF: The base value transition changes occurs due to the change in single transition of the neighborhood cells.[5]

III. Proposed Methodology for ANPSF Testing

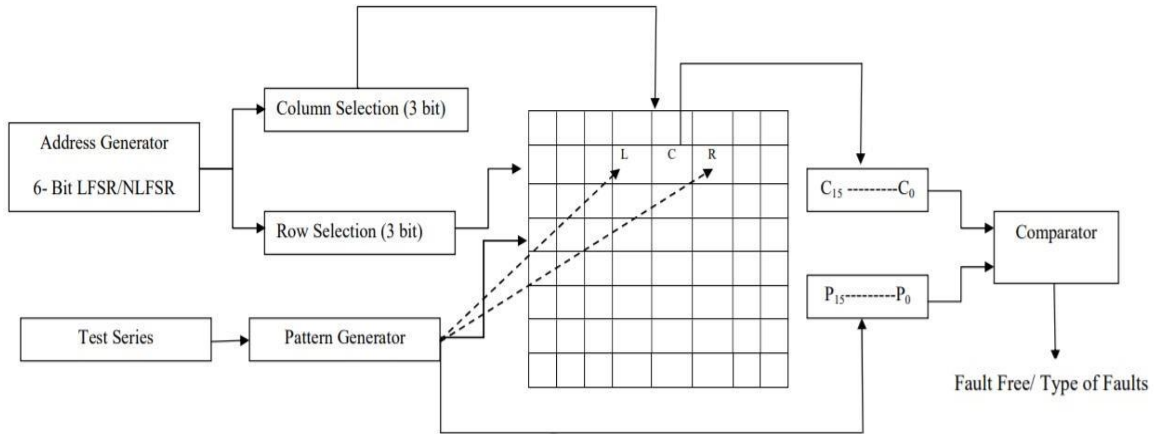

Fig.1 ANPSF Proposed Method

Linear Feedback shift Register

In Digital circuits a shift register is a type of sequential logic circuit, mainly for storage of digital data. A LFSR be a shift register whose enter bit is linear characteristic of its preceding state, the LFSR usually used linear characteristic of single bits is exclusive-or (XOR).[6] LFSR has a well-chosen feedback function that can produce a sequence of bits that appears random and has a very long cycle. The LFSR have to be initialized, with seeded nonzero value. This can be constructed from simple shift registers with a small number of exor gates and mainly used for Random number generation, counters and error checking and correction [6]. The advantages of LFSR are it has a very little hardware and high- speed operation.The LFSR can be constructed from a degree n primitive polynomial.

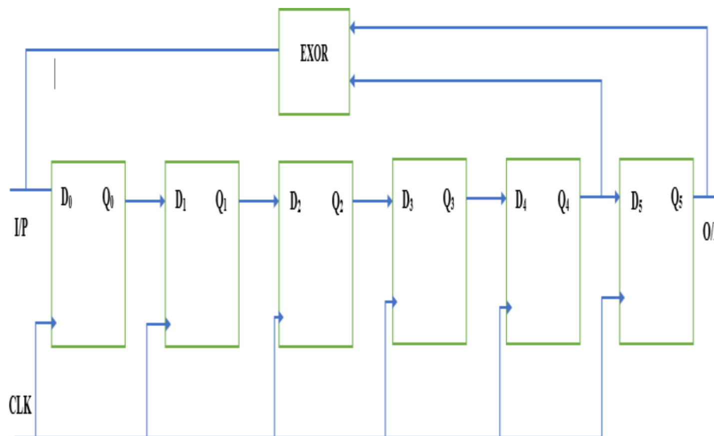

Fig.2 Block Diagram of LFSR

Non-Linear Feedback shift Register

A Non-linear feedback register (NLFSR) is a shift register whose enter bit ought to additionally be a Non-linear characteristic of its preceding state. The NLFSR gives correct fault coverage when evaluate to LFSR. It consumes low power when evaluate to LFSR. The NLFSR can be constructed from a degree n primitive polynomial [6].

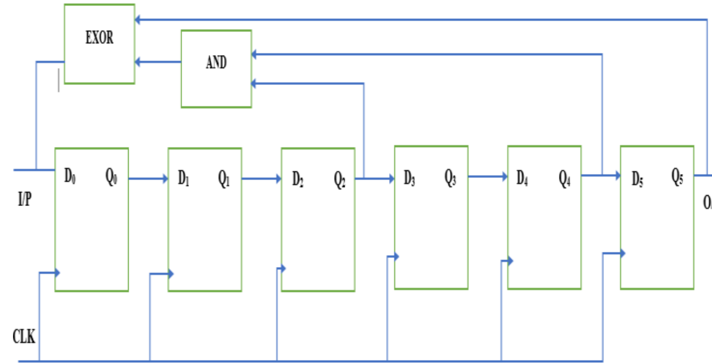

Fig.3 Block Diagram of NLFSR

A. ANPSF Architecture

The figure of ANPSF illustration, LFSR/NLFSR procures an ordered arrangement being address beacon to write/read data into memory.[7] The LFSR/NLFSR is used as an address generator for selection of row and column of the memory. When write_read signal is high the address registered with the patterns from the chosen sequence is drafted in to 3 type neighborhood cells.[8] When the write_read signal is low the input sequences are generated from the selectionof row and column, A negligence patterning may take place, if there is a conversion of base cell on detected of any transition on the deleted local cells. The output of middle bits from the memory and the input centrebits are compared using the exor. The comparator determines that the output is fault free or types of faults (Active faults).

IV. Simulation Results For LFSR

The simulation results for testing the memory for detecting the ANPSF faults.

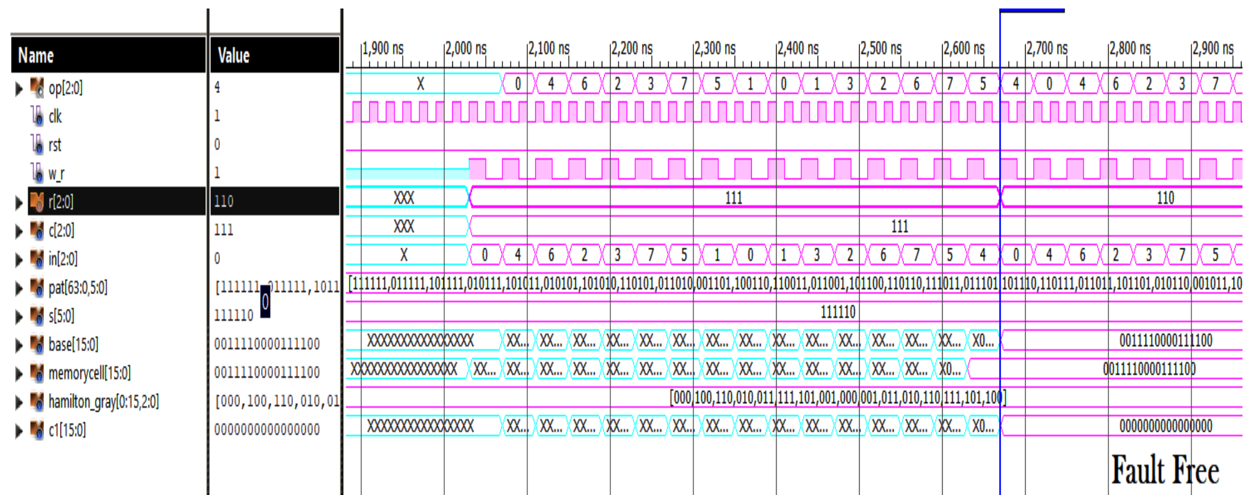

Fig.4 ANPSF Fault Free Identification of Fault free condition by showing all the C1 register values 0000000000000000.

Active Left Faults (Hamiltonian Sequences)

When there is a rise transition take place in the sequence of the left bits 000 to 100, the base value changesto 0 as 1.011 to 111, the base value changes to 1 as 0.

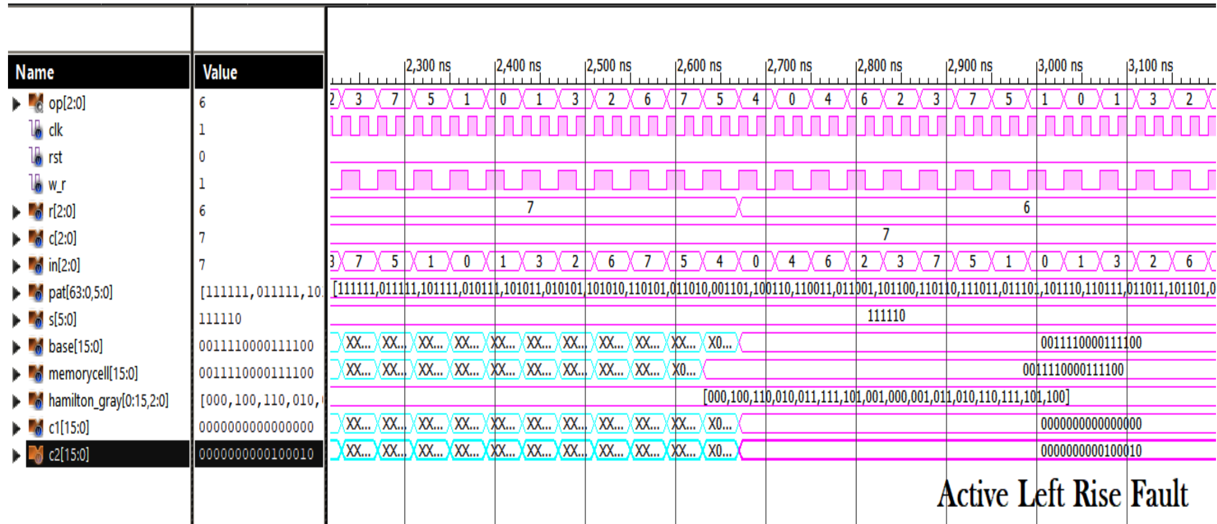

Fig.5 Identification of Active Left Rise Fault by showing the change in C2 as 0000000000100010.

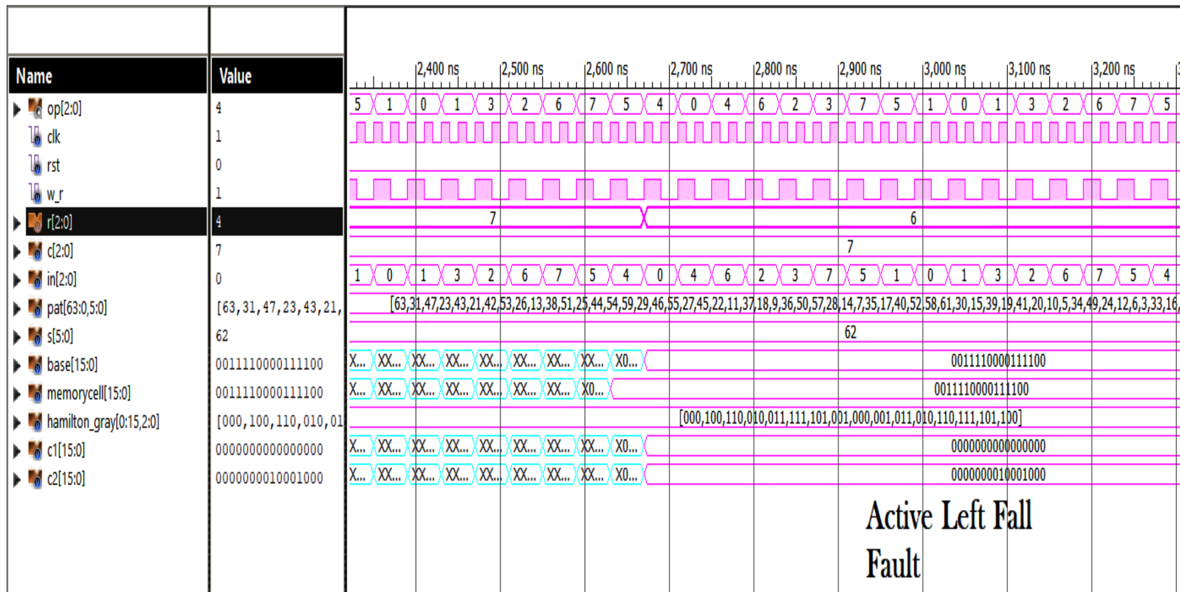

Fig.6 Identification of Active Left Fall Fault by showing the change in C2 as 0000000010001000.

A. Simulation Results For NLFSRActive Right Faults (Gray Sequences)

When there is a rise transition take place in the sequence of the right bits 000 to 001 the base value changesto 0 as 1. 110to 111, the base value changes to 1 as 0.

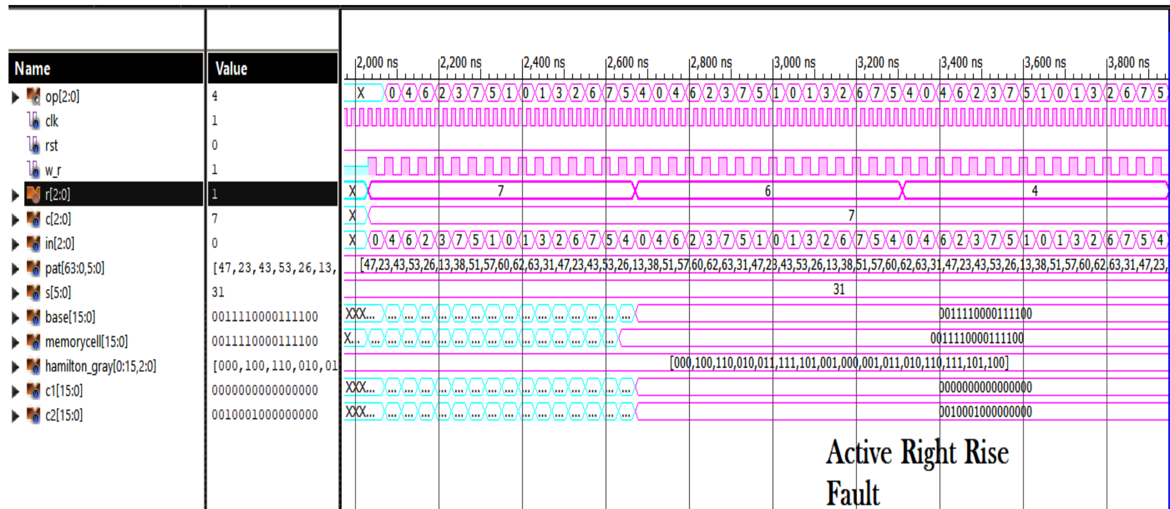

Fig.7 Identification of Active Right Rise Fault by showing the change in C2 as 0010001000000000.

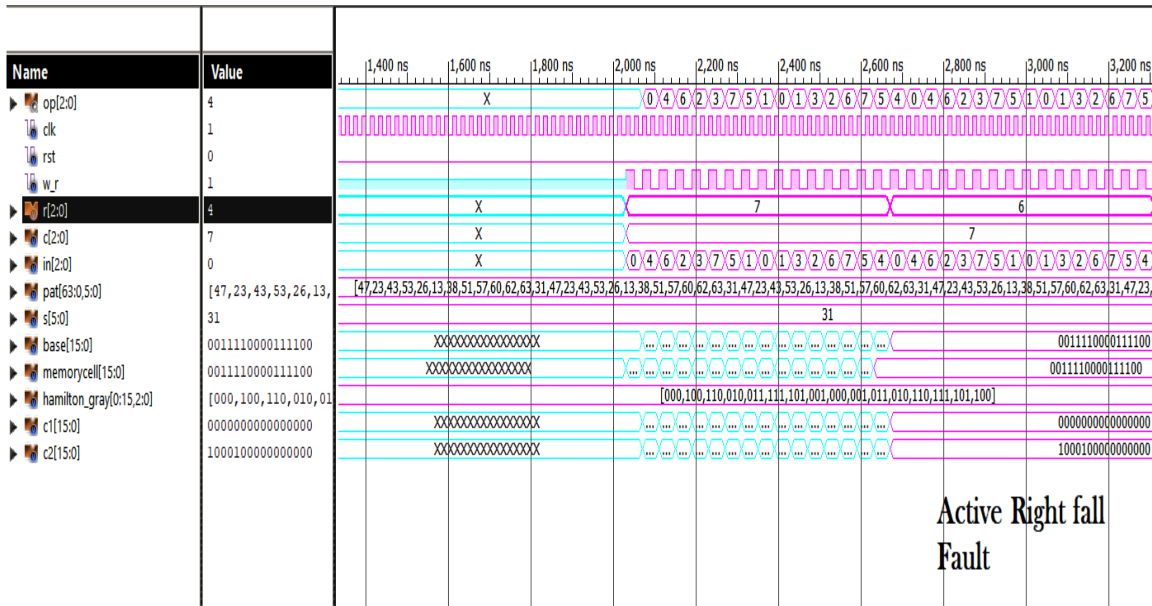

Fig.8 Identification of Active Right Fall Fault by showing the change in C2 as 1000100000000000.

B. FPGAImplementation of Memory

If row=5, column=4 when w_r=1 input=110,w_r=0 output=110 are shown below.

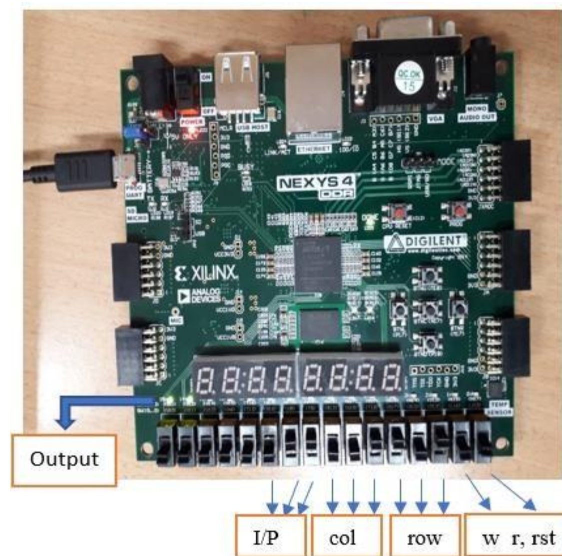

Fig.9 FPGAImplementation of Memory on NexysArtix 7 FPGA

If row=5, column=4 when w_r=1 input=011, w_r=0output=011

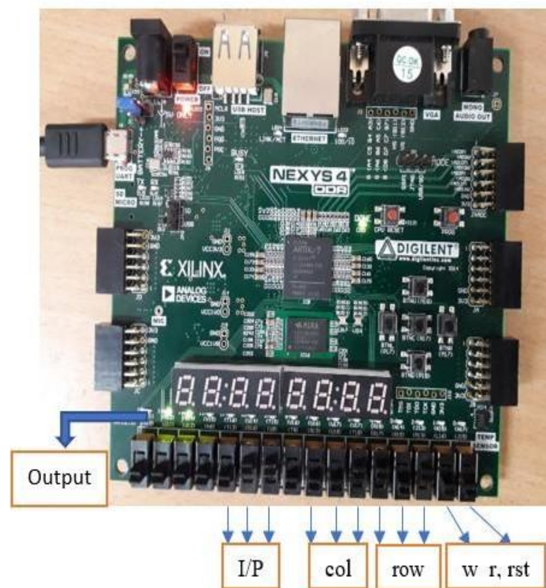

Fig.10 FPGAImplementation of Memory on NexysArtix 7 FPGA

C. Synthesis Report

The synthesis report of ANPSF fault is generated using Xilinx ISE tool.

Parameters	Device Utilization
Slice Registers	37
Flipflops	37
Slice LUTs	69
Occupied Slices	45
LUT Flipflop pairs	72
Fully used LUT pairs	34
Clock Period(ns)	1.921
Maximum Frequency (MHz)	520.874
Input Arrival time(ns) before clock	1.538
Output Arrival time(ns) after clock	0.746

V. Conclusion

Random testing of Three cell NPSF testing is performed in this paper. LFSR and NLFSR are used as address generators to select the particular cell in the memory, Hamiltonian and gray pattern is applied as test pattern on the cell. Read the centre cell value from the memory, and determine the type of fault as per the bit positions of the centre cell. The testing operation is implemented using Artix seven FPGA board.

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