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Research Article

Fpga Implementation Of 4-Bit Alu Using Reversible Logic Gates

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Abstract

The adders, multipliers are the essential building blocks for every integrated circuit (IC). Thus, the design of adders and multipliers must inhibit the area, delay and power efficient properties. But most of the CMOS based logic gates arefailed to provide these properties in adders, multipliers implementation. To solve this problem reversible logic gates has been developed at nano technology level usingthe quantum dot cellular automata properties. The quantum cost for this reversible logic gates very low, thus in this paper reversible logic gates-based 4-bit adder, 4-bit subtractor, 4-bit multiplier and 4- bit ALU developed with reconfigurable properties. The effective utilization of these gates provides more flexible nature for ICs. The implementations are conducted in Xilinx ISE environment, the simulation results shows that proposed method is area, power and delay efficient compared to the conventional approaches.

Keywords*:* Reversible Logic Gates, RippleCarry Adder, Array Multiplier.

INTRODUCTION

The digital computer performs operations that seem to discard data in computer's history. In this, the machine state will be ambiguous [1]. The operations of computers incorporated to overwrite/erase the data and also consists a section which addresses a bitof data addressed at distinctive transfer instructions. Hence, the system is logically irreversible - its transition work lacks a single-esteemed inverse [2]. In developmentof nanotechnology, which is speed enhanced, less sized, and composed of highly convoluted engineering design than existing systems. The improvement in the technology has introduced a system considering the parameters like power and heat dissipation and clock frequency [3].The highly enhancement in the clock frequency to get the better speed and increase the total transistors stuffed in a chip to accomplish required system results more power consumption. Almost in all the total logic gates for logical operations in old computer are irreversible. Hence, in every time a logical operation is performed to know input lost and it is dissipated as heat. For any digital design, the power loss must be considered for desired parameter [4]. The current technology improvement in the computer design are increased and also the power utilization also optimized by using the Reversible

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logic (RL). As per literature with exponential development of heat produced because of information loss is major issue. The heat dissipation causes the reduction in the circuit‟s execution time and lifetime. Thus, the use of reversibility can give low power consumption and heat dissipation system. In the work of literature indicated how the reversibility can be achieved with zero power dissipation. Also, reversibility cannot cause information loss as like in irreversible. For reversibility circuit design we need set of reversible gates (RGs) and these kind of gates are available since last decades. As per literature [7] focused on logical irreversibility which causes more heat losses. Accordingly, a computer must dissipate entropy (kTln 2) of energy for each data loss. An irreversible computer can made reversible by conserving the information. The reversible machine additional unit is used to store the every operation performed. In this machine the controls both the input and output information. Thus, as discussed in [7], this will prevent the information loss as it can be reused. Thus reversible computer halts the information, can be erased in middle results, the output can be reused as input. The research starts with the concept of reversibility [7] where at the ending of computation and first inverse of the transition work, the system can perform reverse computation. The Reversible circuit (RC) can create output from every input, i.e., there is a coordinated corresponding to input and output vectors. Thus, in a RC outputs will be equal to inputs. A circuit can be "reversible", when the input vector is uniquely recouped by output vector corresponding to input and output unit. The RL is a promising design paradigm offers efficient to design the computers with power dissipation. The RL can improve the standard of computing system. The reversible processing fundamentals are the relationship among entropy, heat transfer in a system. The RL guidelines the objective (reversible) device with equal lines of input and output delivering a processing domain. The work of Yugandhar, K., et al [8] gives a new design method for array multiplier which uses more garbage outputs. Authors considered the 4-bit reversible high performance array multiplier (RHPAM) with reversible high-performance adder (RHPA) synthesizing by utilizing the advanced bi-directional synthesis mechanism. Hence, for multiplier synthesis, the optimization of input bits and also the delay are not yet addressed except in the recent works which discusses about the post synthesis mechanism to reduce the quantum bits in the reversible multiplier.

Kamaraj, A., and P. Marichamy [9] introduced the fault tolerant ALU (FTALU) with no input carry with one ancillary input bit. Authors have examined new QR carry adder designs with no ancillary input bit gives improved delay. The reversible ALU in the existing literature is evaluated by garbage outputs, total RL used, QC and delay.

Amirthalakshmi, T. M., and S. Selvakumar Raja [10] have described concepts of 8-bit Reversible ALU (RALU). Also, designed and implemented high cost, efficient, fault tolerant, reversible ALU. In this more garbage outputs were compensated with fewer operations. The author concluded that the ALU performs all the logical operations better than existing methods not arithmetic operations.

Table 1: Summary of Literature survey

Authors	**Problem addressed**	**Outcome**

Yugandhar, K[8]	Synthesis of reversible gates, Adder and multiplier design issues	ALU design with Low QC, delay and garbage output
Kamaraj, A., and P. Marichamy[9]	RL design Reduced minimum outputs	Reduced minimum outputs
Amirthalakshmi, T. M., and S. Selvakumar Raja [10]	Reversible design with sequential circuits	Better design than traditional RL design

To solve these problems, the paper iscontributed as follows

A novel full adder is designed with fredkingate and Feynman gate combinations; this reduces the delay and area requirement.

An N-bit reversible RCA has developed utilizing the reversible fulladder.

An N-bit reversible array multiplier has been developed by utilizing the fredkin gates and N-bit reversible RCA.

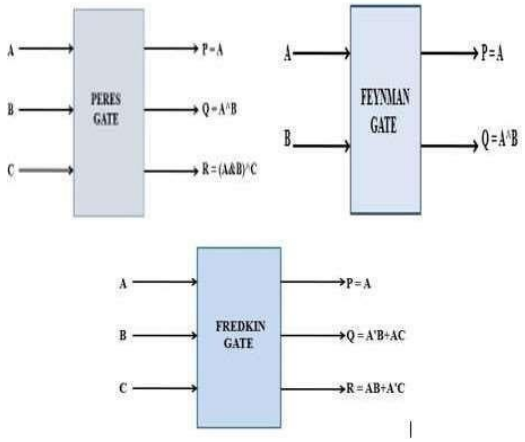
An N-bit Reversible adder subtractor was designed; using this adder subtractor and array multiplier an N- bit Reversible ALU was developed.

A detailed analysis of results has been presented with comparison to the existing method .the results shows that proposed method is area, power and delay efficient.

Rest of the paper as follows: section 2gives the detailed analysis is over reversible logic gates with its unique properties also introduces operations of Feynman gate and Fredkin gate. Section 3gives the detailed analysis of reversible designs such as proposed Full adder, proposed N-bit RCA, proposed N-bit array multiplier, proposed N- bit adder subtractor and N-bit ALU. Section 4gives the detailed analysis on results with respect to both simulation and synthesis outcome and comparative analysis also performed with various convention approaches. Section 5deals about conclusionand future works of proposed methods.

REVERSIBLE LOGIC GATES

Reversible logic gates are developed with the pass transistor technology using quantum dot cellular automata. The reversible logic gates are preferable todesign the chips because they exhibit thefollowing properties.



FEYNMAN GATE: Figure 1(a) gives the detailed operation of Feynman gate, it acts as both buffer and exclusive or gate.

FREDKIN GATE: Fredkin gate is a universal gate, any arithmetical and logical operation can be implemented very effectively with low area, delay and power consumption compared to basic gates. Thus it is effectively used in the ALU operation. The detailed structure of Fredkin Gatepresented in Figure 2(b).

The main applications of Fredkin gate is that, it acts as AND gate as well as OR gate by controlling the input pins. If C input of Fredkin gate is 1'b0, then R output of Fredkin gate acts as AND operation.

$C = 0 \rightarrow R = A\&B + \bar{A}\&1'b0 = A\&B$ (1)

If B input of Fredkin gate is 1'b1, then R output of Fredkin gate acts as OR operation respectively.

$B = 1 \rightarrow R = A\&(1'b1) + \bar{A}\&C = A + A\&C = A + C$ (2)

From the figure 2, it is observed that if Ctrl input is zero, the design acts as reversible Full adder. if Ctrl input is one, the design acts as reversible Full subtractor. And subtraction operation developed based on the twos compliment addition.

PERES GATE: Figure 1(c) gives the detailed operation of Peres gate, it acts as both buffer and exclusive or gate. If the input C is zero, then the outputs R acts as AND function respectively.

PROPOSEDMETHOD

The ALU is the essential building block in every DSP processor DIP processor, Intel processors and all the types of integrated circuits. Thus, the efficient design of ALU makes the design to area, delay and power efficient. In the proposed method majorly focuses on design the 4-bit ALU with combinations of Feyman gate and Fredkin gate, The 4-bit ALU also utilizes the 4-bit Adder, 4-bit subtractor and 4-bit multiplier, thus the operation of each arithmetic unitexplained in detail.

PROPOSED REVERSIBLEFULLADDER-SUBTRACTOR

The design of Reversible full adder and subtractor (RFAS) will be effectively used for the purpose of ALU by utilizing the single architecture for both operations. the twos compliment addition.

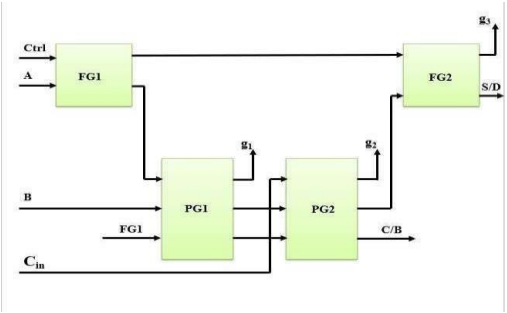
$Ctrl = 0 \rightarrow out = A + B = A + \bar{B} + Ctrl$ (3)

$Ctrl = 1 \rightarrow out = A - B = A + \bar{B} + 1 = A + \bar{B} + Ctrl$ (4)

if ctrl is zero, Feynman gate Fg1 will results the Q output as input A. if ctrl is one, Feyman gate Fg1 will results the Q output as compliment of input A. in both cases, P output such as buffer of Ctrl applied to the A input of Feyman gate Fg2 and Q output applied toA input of pears gate PG1 respectively. Single pears gate is enough to implement half adder or half subtractor depending on it‟s a input and maintaining the C input to Zero. Now, PG1 outputs P1, Q1 will act as half adder sum, carry out when ctrl is zero and similarly act as half subtractor difference, borrow out when ctrl is one. Similarly, Now PG2 outputs P2, Q2 will act as Full adder sum, carry out when ctrl is zero and similarly act as Full subtractor

difference, borrow out when ctrl is one. But as stated above, the design is based on twos compliment methodology, so the final sum or difference contains

compliments so it must be controlled by Feyman Gate FG2.the Feyman Gate FG2contains the inputs as P output from FG1 and Q2 output from PG2. If control is zero, the resultant Q output is Sum and if control is one, the resultant Q output is difference respectively.



PROPOSED 4-BITREVERSIBLE ADDER-SUBTRACTOR

Figure 3 shows the architecture of N-bit reversible adder-subtractor (RAS) consisting of N-number numbers of RFAS, it acts both N- bit reversible adder and N-bit reversible subtractor depending on the ctrl input.

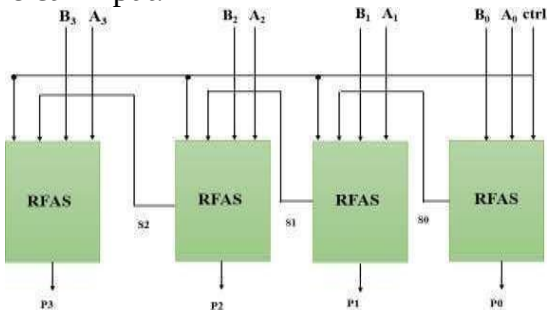


Figure 3: architecture of N-bit RAS

As like RFAS, if ctrl is zero it acts as N- bitreversible adder and, if ctrl is one it acts as N-bit reversible subtractor respectively. The operation of N-bit RAS as follows,

Step 1: individual RFAS generates the sum and bits alone by considering the A, B as present inputs and CB_{in} as carry or borrow out CB_{out} from previous stage. If ctrl is zero, sum and carryout s will generate as finaloutput. If ctrl is one difference and borrow outputs will generate as final output respectively.

Step 2: individual RFAS also generates the CB_{out}, by applying the $CB_{out}$of present stage RFAS to $CB_{in}$of next stage RFAS.

Step 3: by performing the step 1 and step2 operations for N number of stages will develop the N-bit RAS operation with low power, delay and area consumption.

Step 4: By making N as 4, it acts the 4-bit adder and subtractor.

PROPOSED 4-BIT ARRAYMULTIPLIER

The multiplier is the essential building blockin the DSP processor DIP processor, ALUs and all the types of integrated circuits. Thus the efficient design of multiplier makes the design to area, delay and power efficient.

The figure 4 represents the N-bit Reversible array multiplier (R-AM) utilizing these Fredkin gates and N-bit RCA adders.

Step 1: every multiplier consists of partial products as fundamental outcomes. The partial products are generating by performing the bitwise AND operation between A inputs to the B inputs in a chronological order. Here, the PERES gate will be utilized to perform the AND operation as mentioned section 2. For implementing N-bit multiplier, we require N^2 Number of AND operations so that of PERES Gates. After developing the partial products, the partial products are grouped together to perform the multiplication operation respectively.

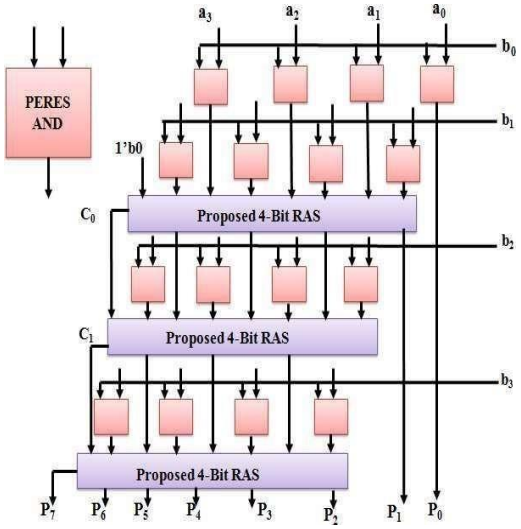


Figure 4: Proposed Reversible 4-bit ArrayMultiplier

Figure 5: operation of R-AM **Step 2:** after developing the partial products,the partial products are groupedtogether to perform the multiplication operation respectively.

Step 3: Figure 5 shows the detailed analysis of partial products addition for 4-bit multiplier. For developing the 4-bit multiplier we require (4-1) number of adder with each of 4-bit

For first 4-bit RFAS(control input is zero so acts as adder) the input will be $M1$, $M2$ and Cin become zero, which generates $S1$ as its sum output and $C0$as its carry output.

3.3 PROPOSED N-BIT REVERSIBLEALU

Fig 6 shows the proposed 4-bit Reversible ALU (RALU) which consist of 4-Bit RAS, 4- bit R-AM and 4-bit reversible logical operations. When selection lines of multiplexer are 3‟b000, then control input for 4-Bit RAS becomes zero and multiplexer selects the adder output, if selection lines of multiplexer is 3‟b001, then control input for

4-Bit RAS becomes one and multiplexer selects the subtractor output respectively. When selection lines of multiplexer are 3‟b010, and then multiplexer selects the N- bit R-AM output such as multiplication. When selection lines of multiplexer is 3‟b011 to 3,,b111, and then multiplexer selects outputs of Bit wise AND, OR, NAND, NOR XOR and XNOR operations generated using Fredkin and Peres gates correspondingly.

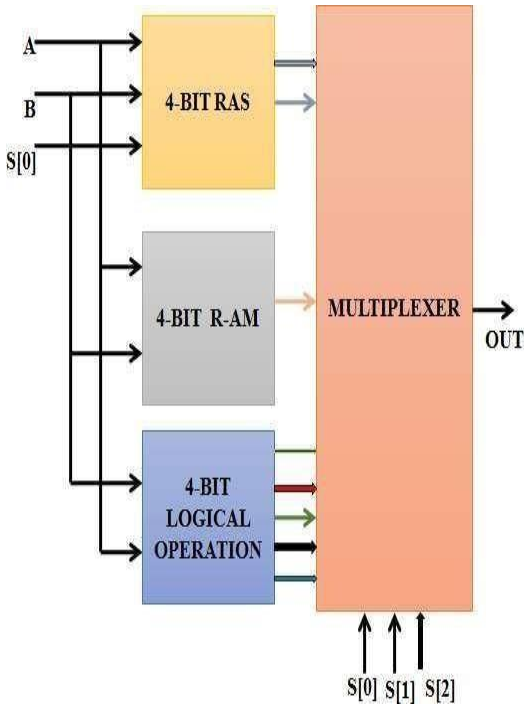


Fig 6: Architecture of4 -bit RALU

RESULTS AND DISCUSSIONS

All the proposed designs have been programmed and designed using Xilinx ISE software this software tool provides the two categories of outputs named as simulation and synthesis. The simulation results give the detailed analysis of proposed design with respect to inputs, output byte level combinations. Through simulation analysis of accuracy of the addition, multiplication process estimated easily by applying the different combination inputs and by monitoring various outputs. Through the synthesis results the utilization of area with respect to the programmable logic blocks (PLBs), look up tables (LUT) will be achieved. And also time summary with respect to various path delays will be obtained and power summary generated using the static and dynamic powerconsumed.

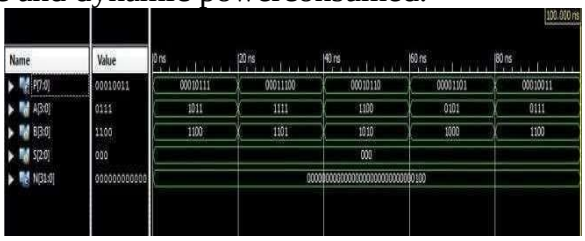


Figure7: Full Adder output

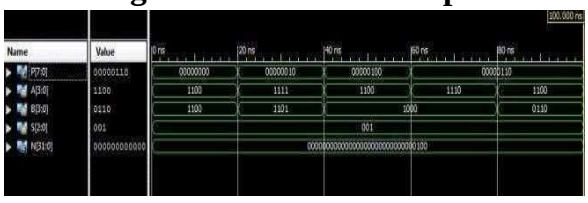


Figure8: Full Subtractor output

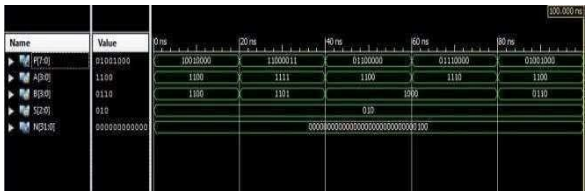


Figure9: 4-bit multiplieroutput

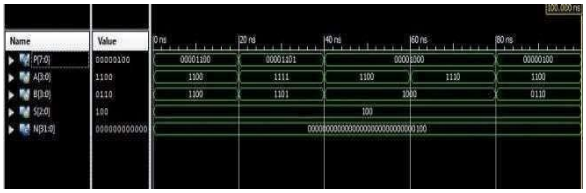


Figure10: Peres And

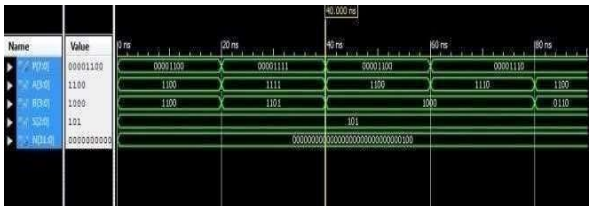


Figure11: Peres Or

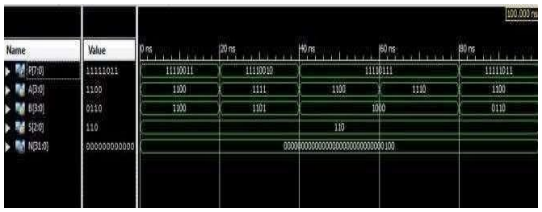


Figure12:Fredkin Nand

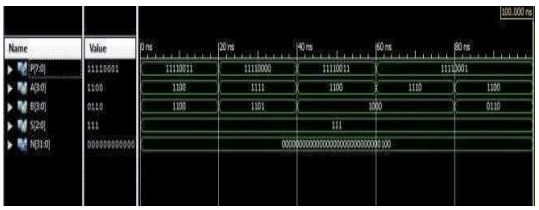


Figure13:Fredkin Nor

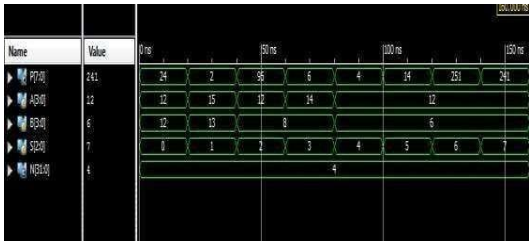


Figure14: ALU Simulation output

Figure 14 represents the simulation output of 4-bit ALU, for various combinations of the input data resultant arthematic and logical outputs are generated based on the selection combinations.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2151	63400	3%
Number of fully used LUT-FF pairs	0	2151	0%
Number of bonded IOBs	131	210	62%

Figure 15: Design Summary

Figure 8 represents the design summary; from this it is observed that the proposed Reversible ALU consumes the less area, lessLUTs.

Figure 9 represents the Time summary, fromthis it is observed that the proposed Reversible ALU consumes the less time with less logical delay and route delay.

Table 2: Performance Comparison

Parameter	**CMOS ALU**	**Reversible ALU**	**%improved**
LUTS	2682	2152	19.7614 % decrease
Delay(ns)	**39.557**	26.859	32.1005 % decrease
Adders/subtractors	**60**	0	NA
Xors	**1947**	6637	NA
BELS	**3427**	2182	36.3292 % decrease

LUT2	**418**	508	21.5311 % increase
LUT3	**312**	43	86.2179
LUT4	**301**	469	55.814% increase
LUT5	**390**	154	60.5128 % decrease
LUT6	**1261**	977	22.5218 % decrease
MUXF7	**34**	31	8.82353 % decrease

From Table 2, it is concluded that the proposed RALU consumes the less area withrespect to XORs, LUTs and it also consumes the less delay as compared to theconventional CMOS ALU respectively.

FPGA IMPLEMENTATION

Figure 16: FPGA IMPLEMENTATION OFRFA

In n-bit reversible full adder when a[0:4]=1

B[0:4]=1; cin=[1] then sum[0:4]=1 ; Cout=1

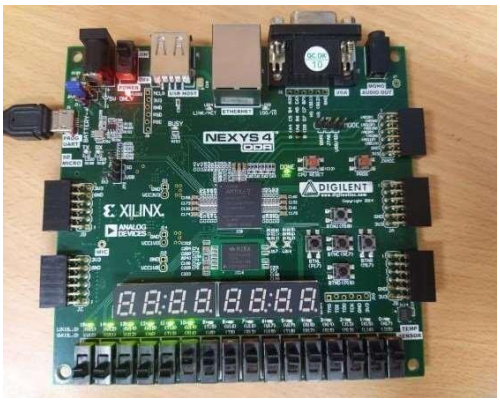


Figure 17: FPGA IMPLEMENTATION OFRFA

In n-bit reversible full adder when a[0:4]=1 B[0:4]=1;cin=[0] then sum[0]=0,sum[1:4]=1 ; Cout=1

Figure 18: FPGA IMPLEMENTATION OFR-ALU MULTIPLIER

In alu 4-bit multipler If a=0 b=0 and selection line=111 then output=11111

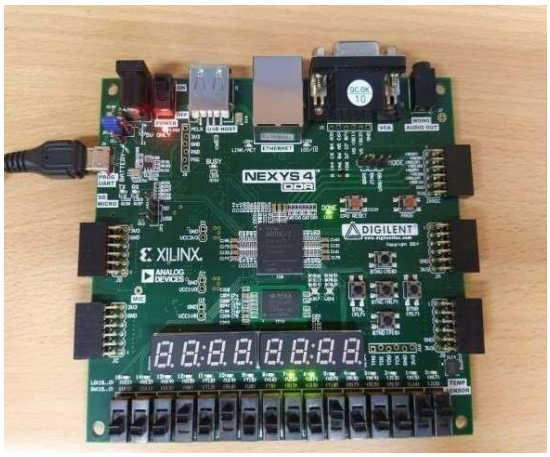


Figure 19: FPGA IMPLEMENTATION OFR-ALU MULTIPLIER

In alu 4-bit multipler
If a=00011 b=00001 and selection line=101Then output=00011

Conclusion

In this paper an area efficient reversible full adder was designed, utilizing this full adder an 4-bit ripple carry adder was developed. And utilizing this 4-bit RCA and fredkin gate an 4-bit array multiplier was developed. Finally common architecture for both adder and subtractor has developed, using this adder-subtractor, array multiplier and fredkin gate an 4-bit ALU has design with low hardware resources utilization. The simulation and synthesis results shows the proposed method has area, power and delay efficient compared to this state of art Approaches and many literatures. This workcan be extended to implement the N-bit sequential logical units such as shift register, counters and so on thus they can be effectively used in every DSP processor and design of any IC achieved through low power ,low delay and area efficient.

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