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Low power High Speed Design of 4BIT Ripple Carry adder using Domino logic

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Abstract
Accurate domino logic circuit keeper control can enlarge the performance, speed. Although, keeper feedback circuit is correlated with the positive feedback gain excessively delay variability is expanded. The main aim is to decrease the delay and reduce the loop gain effect, here domino clock delayed dual keeper (CDDK) circuit is conferred .During the commencing estimation phase, disabled the two keeper devices of the keeper circuit in CDDK domino structure. By decreasing the dispute current concurrently the circuit speed of operation is intensified. The carried out various metrics and outcomes are analyzed for the circuit simulations .Moreover , the simulations are accomplished on a 4-bit ripple adder using structure of CDDK demonstrate decreased characteristics of delay variability due to the domino CDDK structure smaller loop gain in opposition of domino circuit The demonstration of intensified by turn down variance current. Through the counterpart of domino logic circuits in opposition of comparison outcomes are validated. By using this tanner power consumption is around 8 micro watts. The analyzing of circuits is carried out using standard CMOS tanner tool using library of 45nm technology.
Keywords— Domino logic, delay, domino ripple adder low power consumption.

I. INTRODUCTION

Very large scale integration technology [1] is a methodology in which more number of transistors are fabricated on silicon area. In CMOS technology dynamic logic method play an important role in designating more logic circuits. By using dynamic logic method we can optimize more number of parameters related to digital engineering. Dynamic logic methodology plays an important role in VLSI. This will increase the operation of the circuits. To implement dynamic logic circuit on silicon it consumes less space when compare to the static transistor technology. By using this dynamic logic circuits to design any digital circuit it becomes more complicated rather than static transistors. And also to perform it will consume more power. Power consumption by the dynamic logic circuit is more and power delivered to the load is less, if power delivered [2] to the load is less which will decreases the circuit's efficiency. So to enhance the performance of the dynamic logic circuit, and to decrease the delay, to reduce the power consumption. To avoid all stated problems domino logic circuit arrangement is well suited. Due to low noise margin the speed of the domino logic circuit is more compared to static logic gates. In large circuit implementation domino logic circuit operation will play an important role. Which will consumes less space and increased the operation of the circuit compared to the static conventional CMOS circuit. Domino logic circuit arrangement is well suited at integration of more number of circuits on silicon.

Domino addressing a extreme impact in the essential applications of consumption of low power and high-speed [3], like as comparators tag, read out register the paths, programmable encrypt, memories of multiport and SRAM pre-decrypt gate, by the utilization of domino logic style the fan-in gates wide realization is astounding

more, in pull up-network stacking of transistors is avoided .Moreover, prone to rise in the leakage current due to ground collections paths. Fundamentally, domino consists of a transistor MP, restrained by the CLK as in the Figure-1. In the time of CLK LOW state, by making the charge to HIGH Level of the dynamic node, The PMOS act as a charged phase [4]. The pull down network operation fully depends on CLK high level; hence it is called as evaluation phase. From the conventional logic style the domino logic style footer is differential; the footer transistor Mf is discretional .The non-inverted output is provided at the dynamic output nodes by the static inverter, without whisking the problem in driving it facilitates the successive stages. PMOS keeper Mk is incorporates by the domino logic style to refill and HIGH state dynamic node is retained , in opposition to sources of internal noise like sharing the charge which dynamic node is affected and leakage current , which False logic of PDN is evaluated . Moreover , PDN is HIGH state (TRUE) at the dynamic node the charge is discharged across the PDN , to keep back HIGH dynamic node tried by the keeper transistor Mk .This steer to the problems arises among pull down network and keeper transistor [5]. The outcomes in turn down of operating speed. The durability of the circuit improved by the increase in complexity of keeper transistor Mk, which moreover, outcomes in the performance of speed in trading off. That can be proposed as

$$K=W_{keeper}/WPDN$$

Where keeper width is W_{keeper} and the evaluation transistors width is WPDN in PDN arbitrate the circuit durability .Additionally, the device characteristics extremely are pretentious by the inter-die variations and intra-die . The variations in the parameters of the device, like tox and cox lead to changeability in the characteristics of circuit, and they resentfully influence the circuit delay characteristics. The Keeper circuit in the topology of the domino circuit is correlated with loop positive feedback in addition the delay changeability aggravates .Therefore, furthermore to the characteristics of high-speed and consuming low power reduced the loop gain [6].

II. LITERATURE SURVEY:

CMOS circuit logic is an arrangement it is constructed with two networks those are pull up network and pull down network. Pull down network is an arrangement in which PMOS transistors are arranged near to VDD supply. Pull up is an arrangement [7-9] in which always connect the circuit to VDD or High voltage. Pull down network is an arrangement in which NMOS circuit are connected to Gnd. Pull down is a arrangement in which always transistors are connected to ground. CMOS arrangement is combination of Static and dynamic. Static CMOS is a technique it is arranged by PMOS and NMOS transistors. But due to static arrangement area occupied to any logic design is more, and power consumption is more. Due to high power consumption, the static CMOS circuits operation is decreased.

To design more numbers of circuits on single silicon die, domino logic arrangement is well applicable. By this arrangement noise interference is less, due to less noise interference, the circuit operation will increase. Due to this high performance the domino circuit gain is increased. Domino logic circuit performs 2 times higher than static logic design [10] due to lower input capacitance for same output current.

This paper is arranged as I. Introduction. I. literature survey

III. Experimental results. IV. Conclusion.

METHODOLOGY

In arithmetic logic units is a basic module which is used to perform various arithmetic and logic operations . to perform ALU operations by using conventional CMOS transistors consumes more power and reduces its speed, because it requires more number of CMOS transistors. Hence to reduces the number of transistors and decrease the delay domino logic is another technique used to reduce the total number of transistors, by this performance of the transistors is increased a lot. Hence in this paper proposes a 4bit ripple carry adder using domino logic unit

DOMINO LOGIC MODULE

Domino is technique in which cascading of logic gates are arranged. To enhance the speed of the CMOS Static circuits domino logic play important role. This will increase the speed and decrease the delay associated with transistors. Mainly domino is a technique designed to enhance the speed. With this avoiding the problem of cascading. Domino is an arrangement in which PMOS transistor is connected to pull up area and NMOS transistor connected [11] to pull down area. Both the transistors gate is connected to clock. To avoid delay we connect keeper arrangement with inverters and some PMOS transistors.in this paper domino arrangement are

designed and simulated in CMOS tanner45nm Technology. In this analyzed domino with 1. And gate2. OR Gate 3. XOR gate 4. One bit full adder.5. 4 bit ripple carry adder

III. EXPERIMENTAL RESULTS

A.DOMINO AND GATE DESIGN

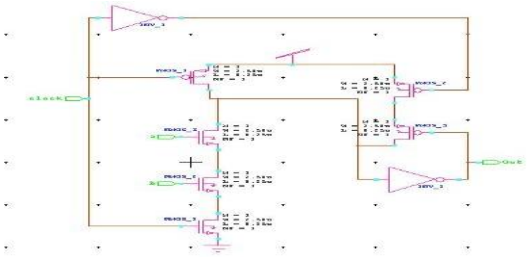

Figure 1. Domino AND gate Schmatic

The above figure shows the schematic of domino logic AND gate.It consists of four NMOS named mn1,mn2,mn3,mn4 and two PMOS named mp1 and mp2.mn1 and mp1 are connected to clock .mn2 and mn3 are connected to inputs a and b.The output is connected to mp2 and mn4.VDD is connected to mp1 and mp2.Ground is connected to mn3 and mn4.

Simulation results :

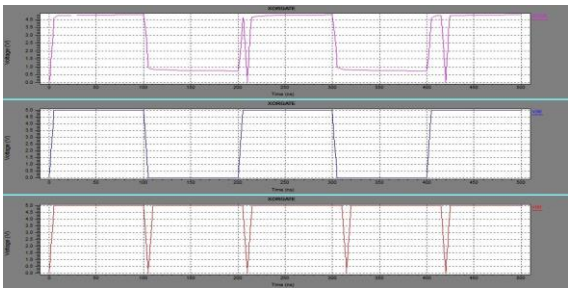

Figure 2. AND gate simulation Using domino logic

For the domino and gate the clock is connected to the mn1 and mp1.When the clock is connected the transistors will get on.When the inputs are given as A=0 and B=0 the output will be 0. When the inputs are given as A=0 and B=`1 the output will be 0. When the inputs are given as A=1and B=0 the output will be 0. When the inputs are given as A=1 and B=1 the output will be 1.

B.DOMINO OR GATE DESIGN

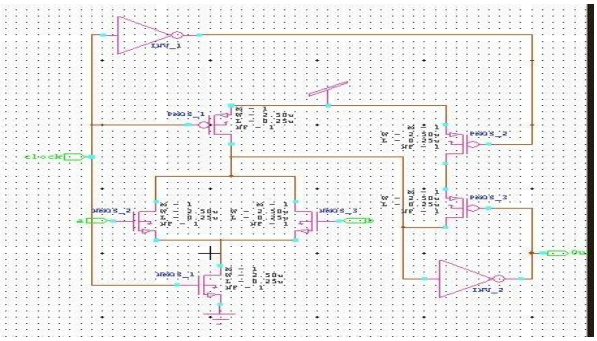

Figure 3. Domino OR gate Schmatic

The above figure shows the schematic of domino logic OR gate.It consists of four NMOS named mn1,mn2,mn3,mn4 and two PMOS named mp1 and mp2.mn1 and mp1 are connected to clock .mn2 and mn3 are connected to inputs a and b.The output is connected to mp2 and mn4.[12]VDD is connected to mp1 and mp2.Ground is connected to mn3 and mn4.

Simulation results :

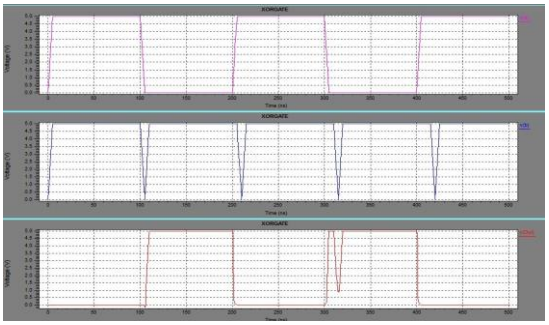

Figure 4. OR gate simulation results

For the domino OR gate the clock is connected to the mn1 and mp1.When the clock is connected the transistors will get on.When the inputs are given as A=0 and B=0 the output will be 0. When the inputs are given as A=0 and B=`1 the output will be 1. When the inputs are given as A=1and B=0 the output will be 1. When the inputs are given as A=1 and B=1 the output will be 1.

C.DOMINO XOR GATE DESIGN

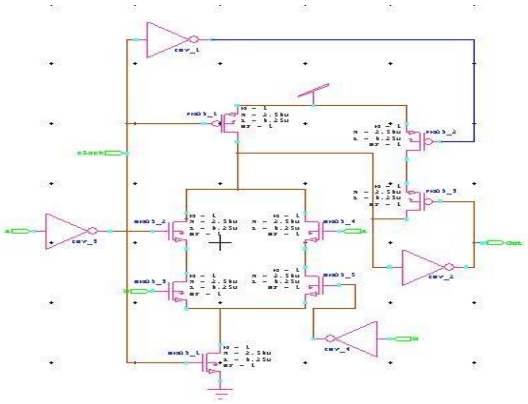

Figure 5. Domino XOR gate Schematic

The Standard domino XOR gate requires two phase input signals,one is original and other one is inverted signal.it needs additional inverters to meet the system design requirements.The two inputs are given to the transisters and we will check the output at output transister pair

Simulation results :

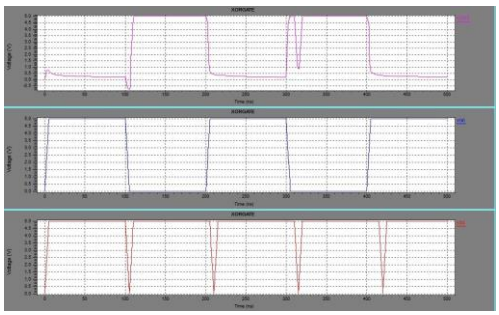

Figure 6. XOR gate simulation results.

For the domino XOR gate the clock[13 is connected to the mn1 and mp1.When the clock is connected the transistors will get on.When the inputs are given as A=0 and B=0 the output will be 0. When the inputs are given as A=0 and B=`1 the output will be 1. When the inputs are given as A=1and B=0 the output will be 1. When the inputs are given as A=1 and B=1 the output will be 0.If the inputs are in the combination of 0 and the output will be 1.If the both inputs are same the output will be 0.

D.DOMINO FULL ADDER DESIGN

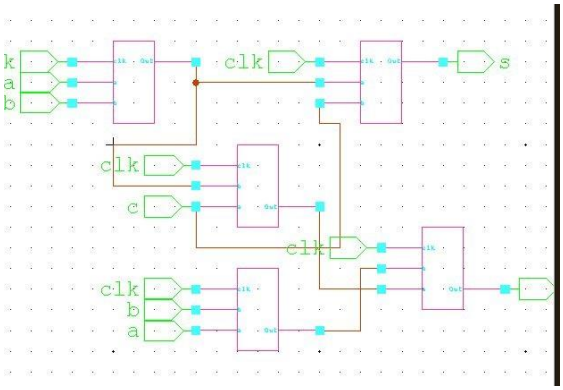

Figure 7. Domino Full adder gate Schematic

The full adder is the basic structure for any arthematical circuit design a,b,clock are the inputs &outputs are sum and carry. In the circuit there is no direct path between VDD and GND .The discharge of the transistor depend on the clock signal .During the precharging clock is low and dynamic node is charged .

Simulation results :

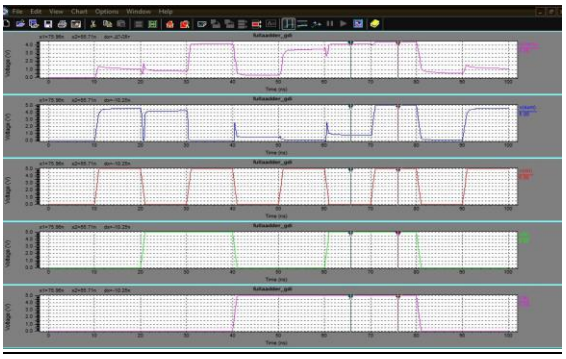

Figure 8. one bit full adder simualtion results

The output shows all possible combinations of 1's and 0's .The 1's and 0's for output variables are determined from the arthematic sum of the input bits .When all input bits are 0 the output is 0.The S output is equal to 1 when only one input is equal to 1 or all the three inputs are equal to 1.The c output has carry of 1 if two or three inputs equal to 1.

4-BIT RIPPLE CARRY ADDER

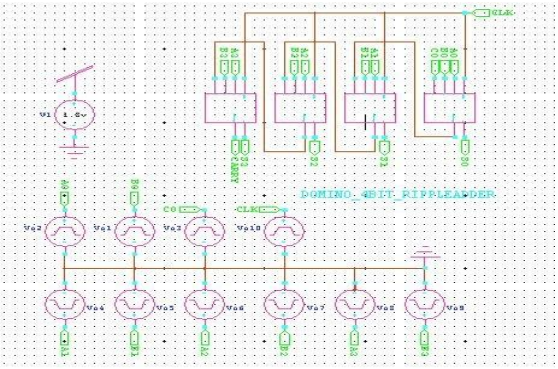

Figure 9. Domino 4 Bit adder schematic

Using ripple carry adder this addition is carried out as shown as shown by above figure.Ripple carry works in different stages each full adder takes the carry-in as input and produces carry out and sum bit as output .The carryout

produced by afulladder serves as carry in for its adjacent most significant full adder .When carry [14] in is available to the full adder it activates the full adder after full adder becomes activated it comes into the operation.When cin is fed as input to the full adder A it will get activated [15] .When c0 is fed as input to the full adder B it will get activated.When c1 is fed as input to the full adder C it will get activated.When c2 is fed as input to the full adder D it will get activated.

Power analysis

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Power Results
VV1 from time 0 to 5e-008
Average power consumed -> 8.384056e-006 watts
Max power 8.384056e-006 at time 4.6875e-008
Min power 8.384056e-006 at time 0
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FIGURE 10: power analysis of 4 bit Ripple carry adder

The above shows the average power consumption using domino logic for 4 bit ripple carry adder is 8.38 micro watts.[16] Hence it’s a best method to optimize the logic circuit using domino.

Table1: Comparison table

The above table 1. Shows the comparison of static and domino logic circuits behaviors.

Sr. No.	Circuits	Static CMOS Logic		Domino Logic using CMOS Tanner 45nm Technology.	
		Transistor Count Delay	Power Dissipation	Transistor Count Delay	Power Dissipation
1	Inverter	2Ps	8u	1 Ps	2.5u
2	AND	2Ps	16u	1 Ps	9.1u
3	OR	15Ps	22u	8 Ps	19.25u
4	XOR	18Ps	34u	12 Ps	20.1u
5	1 BIT FA	20Ps	50u	15 Ps	23.5u
6	4bit ripple adder	25Ps	120u	18 Ps	8.38u

4. Conclusion:

Domino logic is a digital module, which is used to reduce the delays in all digital engineering. In This paper all the modules are simulated using CMOS Tanner 45nm Technology. With CDDK technology [17]. By this technology delay has reduced more, which will increase the rise time and switching speed. With CMOS Tanner 45nm Technology power consumption by the domino logic reduced drastically and increased power delivered to the load increased more. Hence this paper proposes the domino logic module to design all digital electronics modules.

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