Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 6, July, 2021: 8856 - 8865

Low Power High Speed GDI 4-bit RCA Circuit design using 45nm CMOS Technology

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Abstract
In Digital Engineering, if we want to design a 4Bit adder which is very essential component in an arithmetic logic circuit (ALU) and also plays a crucial role in all the computational circuits as well. In this paper, 4 bit ripple adder using a one bit full adder is designed at 45nm CMOS technology.to design a full adder, we require XOR, OR, AND logic gates, where we combine all the above logic gates to get a one bit full adder finally. The GDI (gate diffusion input) it is a technique in which number of transistors required to design specific application will gradually reduce. When it is compared with the conventional circuit.by using GDI not only reduces transistors count but also power consumption The maximum power saving is of 93.04%, the delay is saved by 76.76% and coming to the overall PDP the saving is of 96.01%. By considering 4- full adders we can build a 4-bit ripple carry adder. Hence the whole designing can be done at supply voltage 1.8V as we are using 45nm CMOS technology.
Keywords— GDI Technique, OR gate, ANDgate,1 FA, 4 bit RCA, low Power consumption.

I. INTRODUCTION

Day by day electronic portable systems based on the battery usage demand is increasing, for driving the devices which are portable they require battery. In designing personally communicating devices, mobile phones, laptops and notebooks important concern is speed and power consumption. In VLSI technology[1-4] the parameter which plays important role is power consumption. For making circuitry cool we require cooling fan because of reducing battery life and increase in heating due to more power consumption. The cost of the whole system is affected and the battery life because of the more power consumption. Which discussed in the above devices and digital communication devices mostly are used in the applications such as microcontrollers , video and image processing and digital signal processing operated in the different operations multiplication , addition , subtraction . In the adder cells internally the different operations are performed like multiplication, subtraction, addition .In the digital communication devices designing more vital role is played by the one bit adder. Addition operation is performed by integrating the 1-bit full adder cells[5] in multiple of number digital communication devices frequently, the whole system performance is determined by the adder cells and adder cells is the reason which plays an vital role.

The adder circuit performance and dissipation of power is affected due to the increase in the complexity of the circuit and chip area is reduced. To reduce the power dissipation and size of chip in VLSI design the circuit is concerned in low power. In MOSFET technology the number of types of dissipation of power is two types they are dynamic power dissipation and static power dissipation. The parameters which Effects the device of the static power dissipation are reverse - biased junction leakage, sub threshold leakage, gate induced drain leakage and gate direct tunneling leakage of scaling parameters effected majorly. Power of short circuit and switching are mainly considered in dynamic power dissipation. The theoretical calculations of dynamic power dissipation and static power dissipation respectively ps is the product of the leakage current and supply voltage[6]. PD is the product of half of the operating frequency, load capacitance with square of logic voltage swing. The different

adder circuits are analyzed at different levels of frequency either a one frequency level is compared in this paper by using a parameter power delay product (PDP). The power delay product[7] is calculated theoretically as the product of the average power dissipation and delay of the circuit.

II. LITERATURE SURVEY:

To design complex digital circuits[8] or to design complex arithemtaic logic units the role of full adders are more importanat. Because arithematci and logical operations is essential in designing of memorys. Perofrmnece of the memroys and logicial devices are pureley depends on CMOS devices. full adder is a arithematic and logical unit it play a important role in deisgning the digital circuits. A full adder consists of three inputs those are a,b,c and two outputs those are sum and carry. All ready full adders [9]are designed by three models those are conventional model, static energy recovery model, XOR/XNOR[10] based model. By above model performance of the full adders is decreased because of requrinment of more transisitors. In designing of full adder by using conventional model takes 26-28 transisitors are required. In designing of full adder by using static energy recovery model more than 10 transisitors are required. By using static energy recovery model power consumption is more due to utlisation of more number of transisitors,due to more number of transisitors threhold problem will come in the picture i.e output voltage swing problem. Due to voltage swing problem, performance of the staic energy recovery model will produce more delay across sum and carry. To design 4 bit ripple carry adder by above any model leads to more disputes. The delay and power consumption in previous models not only depends on transistor count but also depneds on CMOS technology files, that means channel length. If channel increased the performance of the circuits is decreased. The circuit defintley fcaes power power losses and also it will decrease the performance of the circuit.hence to avoid all problems in 4 bit parallel adder gate difusion input[11] is prposed with channel length of 45nm.

This paper is arranged as I. Introduction. I. literature survey

III. Experimental results. IV. Conclusion.

Methodology: In designing memory modules requires more area on silicon. In arithmetic logic unit the role of 4 bit ripple carry adders is more precisions. To design such a valuable modules with conventional transistors, leads to more power consumption, power dissipation, delay and speed. Hence to avoid such problems in conventional transistors circuit. Need to optimize the transistors parameters like size, hence in this paper gate diffusion input methods has been proposed to reduce the size of the transistors. This leads to reduce the delay and enhances the speed and performance of the 4bit ripple carry adders.

GATE DIFFUDION INPUT (GDI) TECHNIQUE

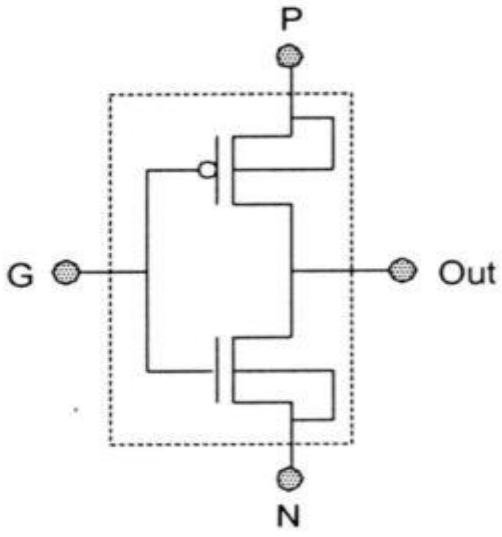

Figure 1. Gate diffusion input model

A low power digital circuit design technique which is used to reduce area, power dissipation, delays and to increase the speed. By this technique circuit complexity is also reduced.
As shown in the above figure it is the basic GDI cell. The basic GDI cell has three inputs. G-common input to both PMOS and NMOS, P&N inputs to source/drain of PMOS/NMOS. The advantage of GDI technique over conventional CMOS technology is that in this technique N, P&G terminals could be given a supply V_{dd} or can be grounded or can be supplied with input signal depending on the circuit to design and hence minimizing the transistor count.

III. EXPERIMENTAL RESULTS

A. CMOS inverter using GDI technique:

As shown in the below figure it is the CMOS inverter circuit using GDI technique. It is designed in 45nm technology. When small voltage is applied the PMOS transistor turns on and NMOS transistor turns off. PMOS will be loaded with the given voltage. As pull up transistor is connected to V_{dd} it will have high voltage and it is pulled up to 5V. [12]Then the value or the signal at the PMOS transistor will be the output. When some voltage is applied NMOS transistor turns on and PMOS transistor turns off. NMOS [13] will be loaded with supplied voltage. As pull down transistor is connected to ground the voltage will be high and is pulled up to a maximum voltage. So, the value or the signal at the NMOS transistor will be the output.

As CMOS transistor [14] has the advantage of interchanging source and drain it can also act as capacitor. If a capacitor connected across the pull up transistor, it gets charged where as if it is connected across pull down transistor it gets discharged as it is connected to ground.
Here the capacitor behavior can be evaluated. The capacitor is discharged and restored but it will not be restored completely because some charge will be held in the depletion region. Here PMOS has the capacity to charge the capacitor to the maximum voltage as the voltage supplied to PMOS is more.

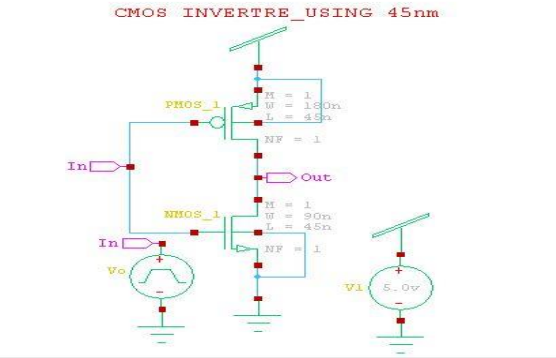

Figure 2. Gate diffusion input using Tanner toll.

B. OR Gate using GDI technique:

As shown below it is the OR gate constructed using GDI technique.

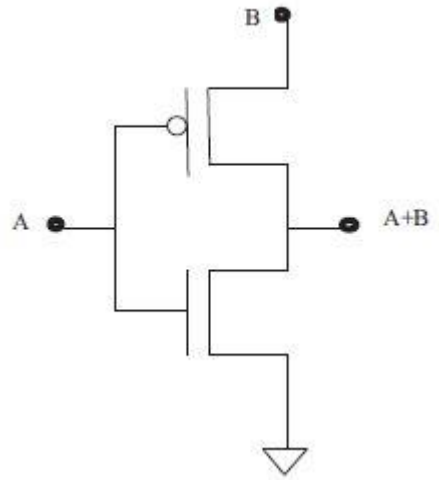

Figure 3. OR using Gate diffusion input.

As shown above, Input A is connected to gate terminal of both NMOS/PMOS transistors. Input B is connected to the source terminal of PMOS transistor and the bulk of PMOS transistor is connected to V_{dd}. Source terminal of NMOS transistor is connected to ground and bulk of NMOS transistor is also connected to ground.

TABLE 1: OR GATE TRUTH TABLE

A	B	Out(Y) = A+B
0	0	0
0	1	1
1	0	1
1	1	1

As shown above it is the truth table of the OR gate. if both inputs are low two transistors turns off and the output will be low. if both inputs or any of the input is high output will be high. If B=0, output Y follows input A (i.e., Y=A) and if B=1, irrespective of input changes output remains same. Using GDI technique number of transistors [15] is reduced compared to conventional CMOS technique.

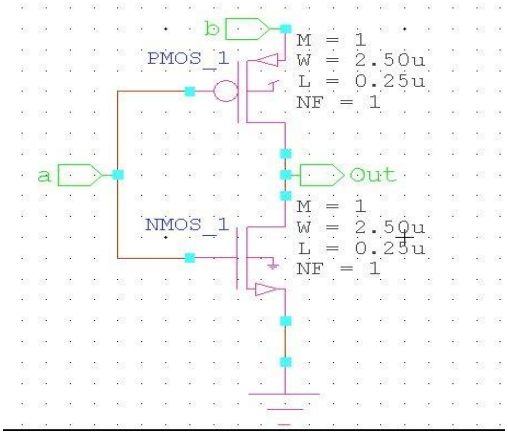

Figure 4. OR Gate GDI Schematic

The above schematic shows the OR gate designed in 45nm CMOS Tanner toll Technology.

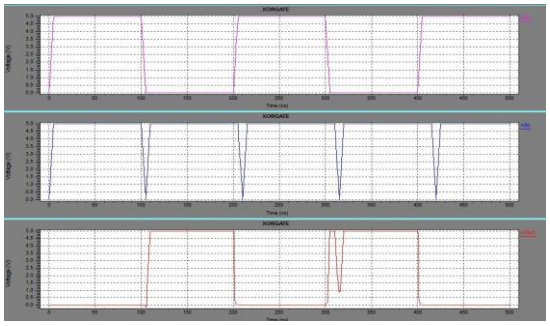

Figure 5. OR Gate simulation results

The above figure shows the simulation results of OR gate using CMOS Tanner 45nm Technology.

C. GDI AND Gate schematic and simulation results

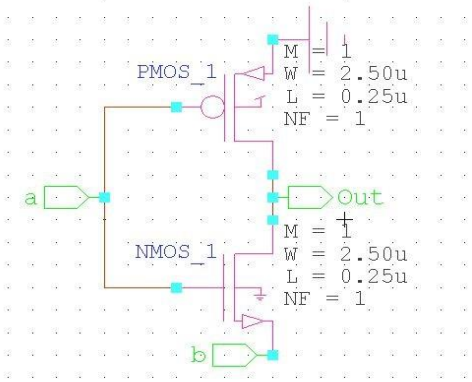

Figure 6. GDI AND gate schematic

The above schematic shows the AND gate designed in 45nm CMOS Tanner toll Technology.

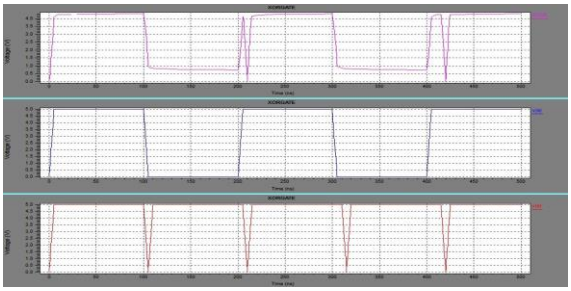

Figure 7. GDI AND gate Simulation results

The above figure shows the simulation results of AND gate using CMOS Tanner 45nm Technology.

D. GDI XOR Gate schematic and simulation results

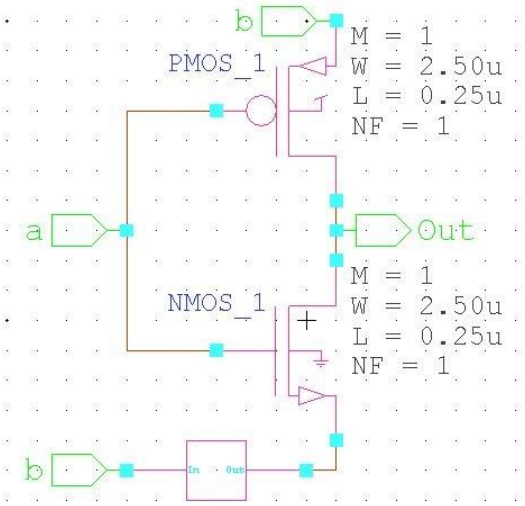

Figure 8. GDI XOR gate Schematic

The above figure shows the simulation results of XOR gate using CMOS Tanner 45nm Technology.

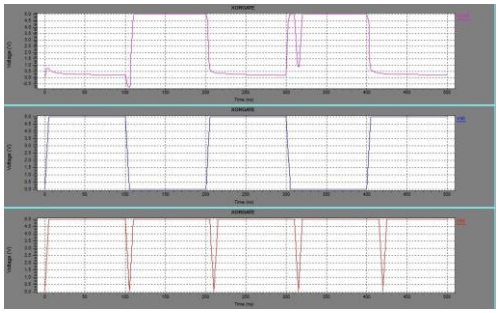

Figure 9. GDI XOR gate Simulation results

The above figure shows the simulation results of XOR gate using CMOS Tanner 45nm Technology.

E. Full ADDER using GDI technique:

As shown in below figure it is the full adder designed using GDI technique.

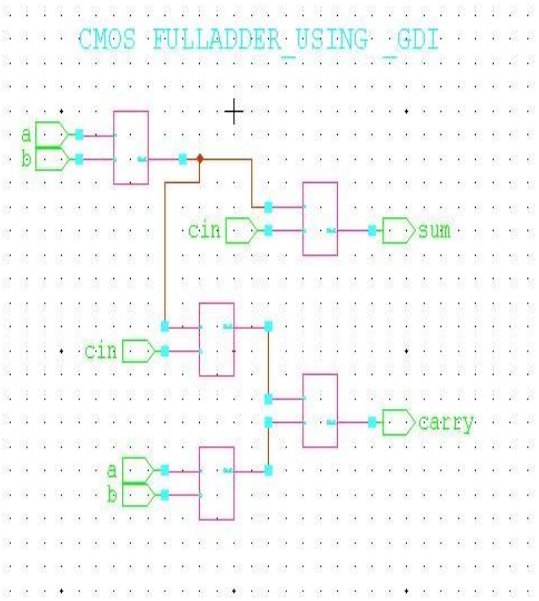

Figure 10. full adder using Gate diffusion input

The full adder is design [16] using less number of transistors using GDI technique.it is a combinational circuit with three inputs i.e., A, B, C_{in} and two outputs i.e., SUM and CARRY.
To design a full adder, AND gate, XOR gate, OR gates are used. As shown in figure inputs A&B are connected to first XOR gate. Output of first XOR gate is connected as one input to the second XOR gate and Input C_{in} is another input of this second XOR gate. Output of this second XOR gate is the SUM. For carry, output of first XOR gate is connected to the input of first AND gate and C_{in} is another input of first AND gate. Inputs A&B are connected to the second AND gate. Outputs of these two AND gates are connected as inputs to the OR gate. Output of the OR gate is CARRY
When all the three inputs are low, both the outputs will be low. If any of the input is high, sum will be high and there will be no carry. If any two inputs are high, sum will be low and carry will be high. If all the three inputs are high, both the outputs sum and carry will be high.
Using GDI technique, area occupied by the full adder is reduced as number of transistors is reduced.

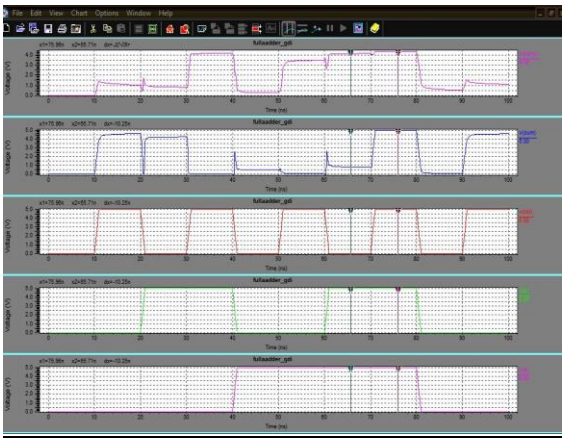

Figure 11. simulation results of one bit full adder

The above figure shows the simulation results of One bit full adder, gate using CMOS Tanner 45nm Technology

F.4-BIT RIPPLE CARRY ADDER

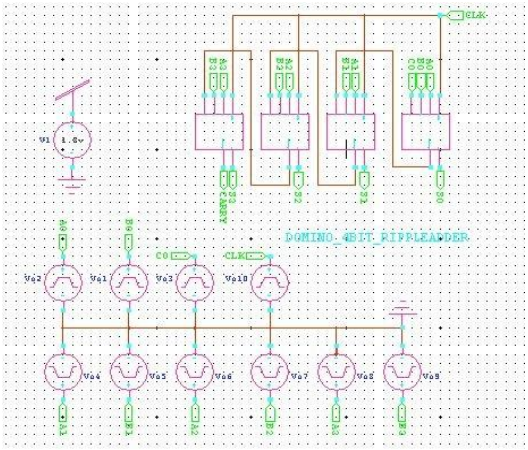

Figure12.Schematic of 4Bit ripple carry adder

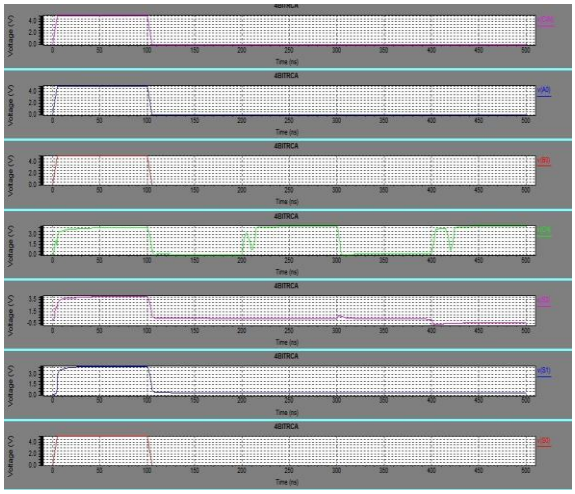

Figure 13. 4BIT RCA output simulation

ripple carry adder is a arithemstic logic unit. The basic bulding blocks of Ripple carry adders are XOR gate, AND gate,OR gate, one bit Full adder[17]. One bit full adders are play an a important role in arithematic logic unit. To design 4 Bit ripple adder four one bit full adders are required. From each one bit full adder sum will carreid out as a output, and each carry will prapogate to next full adder.Ripple carry adder is digital block in which addition of 4 bits is carried out paralley at a time. By adding bits paralley at a time performance of the ripple carry adder is increased up to 50%. To design one bit full adder with conventional model , takes 26 CMOS transisitors. Where as by using GDI Technique 10 Trnasistors are required to implement same performance of the full adder. To design four bit ripple carry adder with conventional model , takes 104 CMOS transisitors. Where as by using GDI Technique all most 40 Trnasistors arerequired to implement same performance of the full adder.

Power analysis:

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Power Results
VV1 from time 0 to 5e-007
Average power consumed -> 3.240000e-012 watts
Max power 3.240000e-012 at time 0
Min power 3.240000e-012 at time 0
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Figure 14. 4BIT power simulation

TABLE 2: Comparison with the previous Methods

Parameter	Average power consumption(-e9Watt)@VDD				
	5V	5V	5V	5V	1.8V
Conventional (112T)	10.63	13.52	17.10	27.27	112.2
SERF (50T)	11.81	14.92	19.51	42.52	311.5
GDI (40T)	59.73	278.3	778.6	1768	3.24e-12

4. Conclusion:

Gate diffusion input is a technique in which all digital logic gates are designed with less number of transistors. By using conventional transistors to design complex digital applications needs more numbers of transistors and also consumes more power, area which reduces speed of the circuits. But these proposed Gate diffusion techniques the performance of the circuits is increased to 90 percentage.

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