Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 5, July, 2021: 4548 - 4554

Research Article

Implementation Of Improved Tcam (Ternary Content Addressable Memory) Based On Parity Bit In Nids System

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ABSTRACT

Network intrusion detection system (NIDS) is developed to identify these network attacks by a set of rules. This paper introduces energy optimized high performance ternary content-addressable memory (TCAM) for Network Intrusion Detection Systems (NIDS). The proposed special-purpose TCAM can analyze the payload data to detect the virus by inspecting only a few bytes. Hence, it adaptively cancels unnecessary searches, leading to greatly reduction in the search delay time and energy dissipation. However, searching for multiple patterns is a computationally expensive task in NIDS. Traditional TCAM solutions cannot meet the high bandwidth demanded in current high-speed networks. Here improved optimized TCAM is used to detect whether an incoming string contains patterns. In this paper, we propose to use an improved version of TCAM in the NIDS (Network Intrusion System) to improve its performance and reduce the power consumption to achieve gigabit performance. In this brief, we propose a novel power-aware reconfigurable FPGA-based TCAM architecture that enables only a portion of the hardware to perform the search operation.

KEYWORDS*:* TCAM, Pipelining mechanism, Gated clock, FPGA, NIDS system etc.

1. INTRODUCTION

Content-addressable memories (CAMs) have different characteristics as compared to all other memories in terms of data processing and associated memory access location. In CAM *search* operations plays vital role irrespective to the type of memory used such as look-up tables (LUT), RAM, ROM and look-up buffers (LUB). As compared to other modes of implementations TERNARY content addressable memories (TCAMs) have become highly popular in many real time applications due to its high speed computations and used predominantly in network packet classification. However TCAM for computationally intensive process like payload pattern matching requires appropriate optimization to accommodate wide range of search in virus databases. The advancements in memory handling rate that have been increased steadily rapidly which leads demands over system design and implementation to support all newly emerging standards. Thus, building a TCAM system that ensures compatible with various data rate demands has gained a lot of interest. As a result, high performance TCAM

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are highly motivated for device modelling due to its flexibility and scalability over other conventional CAM design solutions.

This work mainly focuses the design challenges related to TCAM system implementation for most compatible device model which can support wide range of communication system. This work outlines some of the major requirements of TCAM for next generation packet classification system which includes optimized system architecture, achievable data rate and energy constrains. On other side Field-programmable gate arrays (FPGAs) are emerging as highly flexible core devices due to its low cost and time to market. It has different forms of applications in the field of networking with its inherent benefits of reconfigurability, speedy prototyping, and high-end parallelism.

The paper comprises of the following sections: Section II provides the various optimization over TCAM related work. Section III discusses the proposed TCAM NIDS system. Section IV discussed FPGA implementation results and also provides its performance metrics evaluation and Section V summarize the work.

1. RELATED WORKS

FPGA based TCAM architecture maps the sub blocks in order to avoid the synchronization problem and its computational complexity grows with the data width which is optimized using various partitioning scheme and data mapping models. Mahmood et al., (2018) developed a novel approach to design a ternary content-addressable memory (TCAM) as a replacement to conventional lookup tables and static random-access memory for high performance memory access. Ullah et al., (2018) developed energy optimized pre-classifier-based TCAM mode for final classification stage of balanced data mapping. Results proved that proposed TCAM outperforms conventional SRAM-based implementation. By selectively activating blocks for each incoming data word entire TCAM memory space is optimized.

Ly, Denys RB, et al., (2018) proposed RRAM-based TCAMs to narrow down the trade-off measures that exist between search latency and reliability in pattern matching during match/mismatch detection. Bremler-Barr, Anat, et al., (2018) investigate various TCAM applications in the field of packet classification and showed various optimization models to solve the problems, such as the search problem and its energy variants. Khan et al., (2021) developed memristor-transistor based hybrid TCAM to overcome the limitations of CMOS-based memory circuits. Zhong et al., (2021) carried out TCAM based packet classification using multiple rule-sets and allows multiple matching rule-set to support different network functions. Gupta, Navneet, et al., (2021) developed highly parallel *search* operation and optimized both speed and energy per *search* in TCAM architecture.

Salah et al. [2011] analyzed the performance measures of snort NIDS over normal and malicious network data with different rate conditions. The measures of packet loss encountered at the kernel level and the fine-grained control over the percentage of the CPU bandwidth proves that this Snort NIDS performance is largely depends on processor scheduling. The data processing rate is improved significantly with consequent scheduling and bandwidth extensions. The most generic methods for regular string matching in many NIDS systems used some finite automata (NFAs or DFAs). In [2012] digital system is developed to offload string matching process from NIDS software to reduce the overall system latency. Most commonly used pattern

matching architectures in FPGA systems for regular expressions are NFAs and DFAs. Hardware implementation for fully automated rule set updating process is implemented in [2018].

As stated in Gramlich et al. [2014] Non-deterministic finite automaton states are reused for multiple patterns matching which gives memory efficiency with considerable complexity reduction, and gives only modest throughput. Deterministic finite automaton overcomes the limitations that arise in NFA at the cost of memory space. Pao et al. [2015] presented DFA for multi string comparisons using repeated characters in several NIDS patterns its frequency of occurrence in different rule sets. Memory efficiency can also be achieved through multi-hashing function which is driven by bloom filter. Similarly using graphics processing units for regular expression matching the processing time can be reduced during pattern matching process. By using on chip memories for handling patterns speed is improved considerably.

In some NIDS system scalable intrusion matching is developed in [2020] with highly reconfigurable processing elements. Memory efficiency was achieved through multi-hashing function which is driven by bloom filter. This new architectural changes can match multiple characters for each clock cycle using wide length data bus. The data processing rate is improved significantly with constant operating frequency. The evaluation results showed that this IDS model handles up to 33 Gbps of normal traffic and reaches 9 to 10 Gbps throughput rate even when networks contain full of signatures, and overall 1.9 to 4.3 Gbps performance rate over the existing state-of-the-art software IDS.

Lin et al. [2021] developed hardware efficient *N*FA NIDS system for Regular pattern matching using highly reconfigurable sub-pattern matching units. The hardware resources are shared among multiple regular expressions using infix and suffix sharing architecture and device utilization rate is minimized. Experimental results proved that this NFA model attains data rate of 1.45 to 2.35 Gbps with significant design complexity reduction.

2. PROPOSED NIDS TCAM SYSTEM

The advent of wireless communication, 5G wireless is the key and heart of Internet of Things (IoT) to build network of networks that are interconnected and can be utilized in many applications such as healthcare, e-marketing and remote monitoring etc. The emergence of malicious contents is speculated for different individual's personal gain. To prevent these problems network intrusion detection systems are widely used for network security. Intrusion detection system is a widely used tool which provides the security against various malicious threats in any network. It is act as final defense in network after firewalls as shown in figure 1. Though it is used to monitor the payload packets coming from network as like firewalls its core functionality is most complicated one than task accomplished by firewalls. Firewalls always used to perform data monitoring only by analyzing packet headers where in the case of NIDS system it will check entire payload data to perform filtering by analyzing.

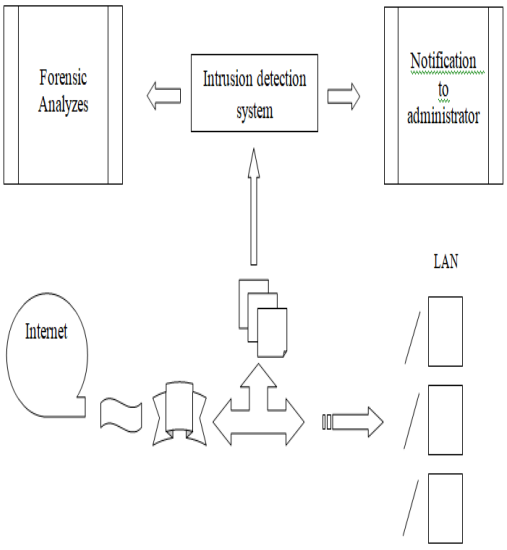

Figure 1: Network intrusion detection system

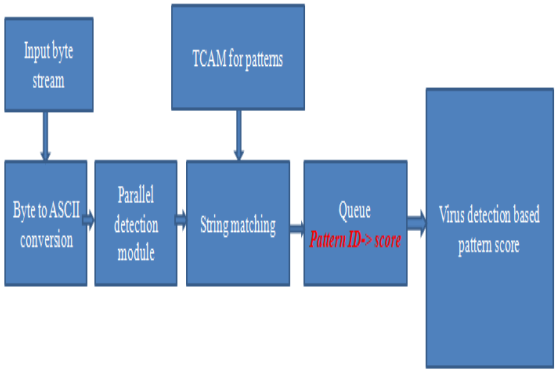

Figure 2: proposed TCAM based packet classification system

3.1 Packet classification

The density of TCAM has improved significantly over the recent years with aggressive CMOS technology scaling. This area and power optimized TCAM as shown in Figure 2 extends its usage in network and classification applications. Packet classification is the basic computational kernel in various network related functions such as network firewall, payload validity and network intrusion detection system (NIDS). By enabling Ternary content addressable memory (TCAM) for performing efficient packet classification full fill the data rate demands of next generation networks. Moreover, by using pipelined TCAM multi modal packet classification is accomplished, which is associated to more than one rule-set.

3. RESULTS AND DISCUSSION

The design is scripted using Verilog HDL file and synthesized using Quartus II EDA FPGA synthesizer with cyclone II family EP3C16F484C6 device. Initially functional verification is done using exhaustive test bench which is driven by payload bit stream. Both variable rate and inherent properties of match constraints are well proved using simulation results. The potential benefits of synchronization and its efficiency over variable rate parallel processing is also proved through simulation results. Here showing some of the outputs taken using Model Sim software and Quartus II software. Further, these results are used to compare the proposed TCAM algorithm with Aho-Corasick algorithm, Deterministic finite automaton and bit level pattern matching algorithm as shown in Figure 3.

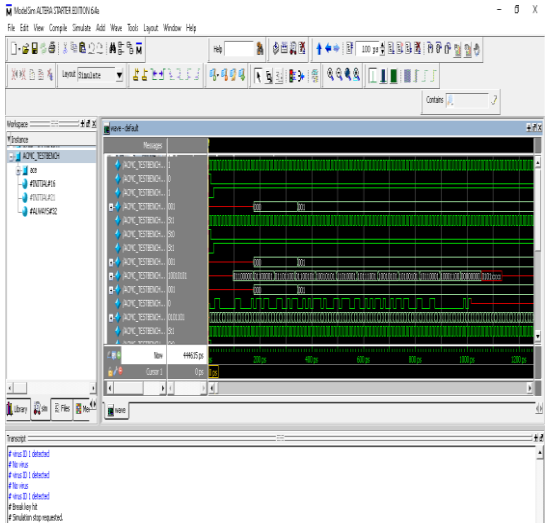

Figure 3:ModelSim simulation report

Here content matching is performed using parity generated selection bits which can optimize the memory banks required for matching process and produce end results with least computations overhead. Here 8 bit data is converted into 2 bits parity selection bits for optimized TCAM as shown in Figure 4.

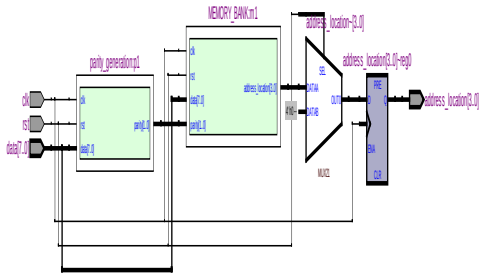

Figure 4:*Parity selection based TCAM schematic report*

Table I Comparison table for TCAM based pattern dividing methods

PATTERN DIVIDING METHODS	AREA SUMMARY	Fmax report	POWER DISSIPATION
Conventional model	184	153.96 MHz	59.51mW
Proposed TCAM	94	674.76 MHz	55.56mW

Here combined decoded TCAM memory with hashing functions is used to achieve data rate up to 8 Gbps as shown in table 1. For every clock cycle new input string is evaluated with linear in time relative to input payload data. The first approach decoded partial Content Addressable Memory (CAM) utilizes some pre-coding technique to share hardware resources which minimize the design complexity. The second method perfect hashing memory reduces the memory utilization rate which regulates the complex memory access using hash function. Additionally, decoded TCAM memory is designed with hashing functions to achieve high date of up to several Gbps. Through this more than one input string can be evaluated for every clock cycle which is linear in time relative to input payload data. Some architectural changes can also be done to match multiple characters for each clock cycle using wide length data bus. The data processing rate is improved significantly with constant operating frequency.

4. CONCLUSION

In this work, a comprehensive statistical framework is developed with parity selection bit generation and gated clock driven low power transformation for high performance TCAM architecture. Initially pipelining approach is used to narrow down the path delay overhead while preserving inherits the statistical parameters. The main focus of this work was to overcome the limitation that arises with existing TCAM model using partial matching techniques. It is started by introducing a high performance TCAM techniques followed by design of appropriate pattern matching techniques using mapping function and simplified arithmetic blocks for NIDS protocol. To validate and proves its applicability, the proposed NIDS system using TCAM was evaluated with different input test patterns and FPGA hardware synthesis.

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