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Research Article

Modified Non Linear State Transistion Based Lfsr Test Pattern Generation For Bist Systems

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ABSTRACT

The LFSRs have been employed as test pattern generator in BIST for decades; however an emerging problem with design constraints leads a lot of improvements in this field. This paper presents a memory efficient FSM encoding-based method to generate test patterns for a given primitive polynomial LFSR TPG. Here test patterns generated from LFSR is divided into groups and follows encoding to transform into multiple test patterns. These newly generated encoded test patterns further divided into transitional and non- transitional blocks which control the bit transitions over encoded values. This weighted driven bit transition also prevents certain bit transitions that reduce the dynamic power as well during testing process. Here highly optimized LFSR test pattern generation is accomplished with high performance TPG design. Extra clocking is also applied to control LFSR output test pattern for improved randomization characteristics of test patterns and pseudorandom measures. The generated random patterns from LFSR are applied to CUT for improved fault coverage using shift and scan method.

KEYWORDS: LFSR, BIST, Fault coverage, Test pattern generation (TPG), FPGA etc.

1. INTRODUCTION

In recent years Built-in self-test (BIST) has been emerged as prominent BIST solutions for many complex circuit systems to improve its system performance by detecting the faults and defective digital components [1]. On the other side testing power consumption reduction is also need to be optimized using some appropriate transition reduction. Energy efficient TPG is emerging as primary LFSR design concern to narrow down the BIST testing power [2-3]. This makes BIST a difficult task to accomplish, which require prominent TPG methodologies. To ensure the BIST systems are economically viable, all intermediate LFSR TPG models should comprised with minimal resources and simplified reseeding computation which makes traditional BIST methodologies [4] out of choice for many CUTs. The inherent data aggregation and information sharing properties render all existing LFSR TPG algorithms impractical.

The major objective of high performance LFSR core is to evaluate, develop, and analyze randomization models used in each stages of BIST in-order to achieve higher fault coverage with

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improved energy efficiency. Among many TPG models, LFSR is the most promising method used for test vector generation in BIST systems and has proven to be an optimal technique well suited for reliable testing process over many CUT models. It can able to support high rate random vector generation and also robust to detect all kinds of faults.

2. RELATED WORKS

In this section includes the advantages of existing LFSR TPG core [5-6] and its implications on BIST measures in detailed. In general working principle and its parametric measures of any LFSR core system are largely depends on pattern length, number of seeds and various polynomial transformation models involved during test pattern generation. In most cases trade-off is made among these measures. Implementation of BIST core in related testing applications are applicable only with some optimization models due to its parametric constraints.

. In [5] BA algorithm and the SB theorem is used to compute the polynomials of LFSR to get 100% fault coverage. However generating LFSR polynomial for selected non-test cubes always required to solve multiple non-linear GF functions in many BIST applications. In [6] developed TPG technology mapping based hardware optimization over LFSR core instead of logic optimization. As a result both the linear and non linear functional blocks of LFSR are considerably reduced, without causing any significant fault coverage. In [7] optimized the LFSR core for lightweight BIST applications and reduce hardware complexity effective and energy consumption. To narrow down computational burden of BIST architectures is analyzed based on CUT design specific hardware analysis for LFSR core. It includes pre coded seeds, the pure polynomial logic implementation using Galois field and the path optimized pipelined version of LFSR. Finally optimal seed computation and LFSR random pattern generator based optimized LFSR core.

In [8] developed high-end BIST implementation based on randomization which exploits parallelization over many-core platforms. The building blocks used on each stages of BIST utilized LFSR approach for parallelization. This improved parallelization offers significant throughput rate. In this new BIST model, the LFSR implicitly handled simple data rearrangement and neglects complex computing process.

Novel LFSR model invented in [9] used self reseeding and dynamic XOR computations. By introducing new mapping measure which comprise of XOR and arithmetic model of modulo n operations for one-to-one mapping function offers several key contributions to BIST structures by activating hard to detect faults.

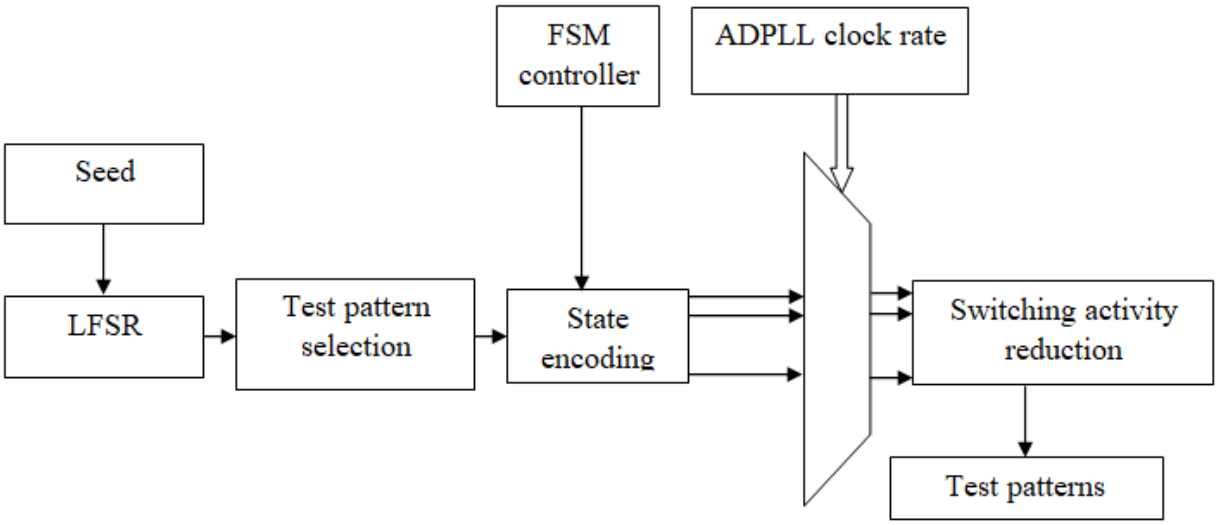

Fig.1. Proposed FSM based multi rate LFSR TPG model

3. FSM BASED LFSR TPG MODEL

Among various TPG methodologies investigated for BIST ALFSRES is considered as a prominent one due to its simplified randomization measures.

- Randomization problem- In BIST the test patterns applied need to be pseudorandom patterns that can be generated typically by a LFSR.

Requirement for PG: High randomness, memory and area efficient implementation.

Requirement for BIST: High fault coverage, detect hard-to-detect faults and low testing power.

- .High performance BIST aims on following requirements
- **Fault coverage demands -** to support wide range of applications.
- **Low power -** to support real time applications.
- **Trade off measure -** to narrow down the penalty gap

Though LFSR is technically advanced TPG core still significant performance tradeoff is always occurs in many real time BIST applications due to its complex polynomial computations. Optimization is essential for LFSR to implement in BIST systems as shown in Figure 1.

3.1 Performance Measures

The attainable fault coverage of any BIST algorithm is largely depends on seed size and associated element of testing operations involved in random test pattern generation process. However randomness enhancements through reseeding come with some significant

computational time and hardware complexity overhead. Different algorithms used different level of complexity trade off to meet desired randomization levels. Multi rate clock based seed mechanism is widely used reseeding model for LFSR randomization measures over other BIST algorithms. In this type worst case reference are used which is formulated from CUT models selected for BIST applications.

3.2 Random Sequence for BIST

LFSR test vectors are always used to describe with some unique discrimination model to explore the unique randomness characteristics of different test patterns. The generic TPG model generates patterns with some invariant features to incorporate the basic characteristics and all other relevant information's useful for testing measures. In real time BIST environments, the vectors are not stable in nature, and the method proposed should accommodate all non linear dynamics of testing processing like struck-at-faults, synchronous faults and dynamic changes etc.

4. EXPERIMENTAL RESULTS

4.1 Simulation Results

In order to validate the importance of FSM controller based random test pattern generation process and to verify its impact in BIST system during testing process is simulated using appropriate test inputs in various stages of data propagation as shown in Figure 2. The potential benefits of FSM in random sequence generation and its efficiency over conventional reseeding LFSR TPG design is also proved through simulation results

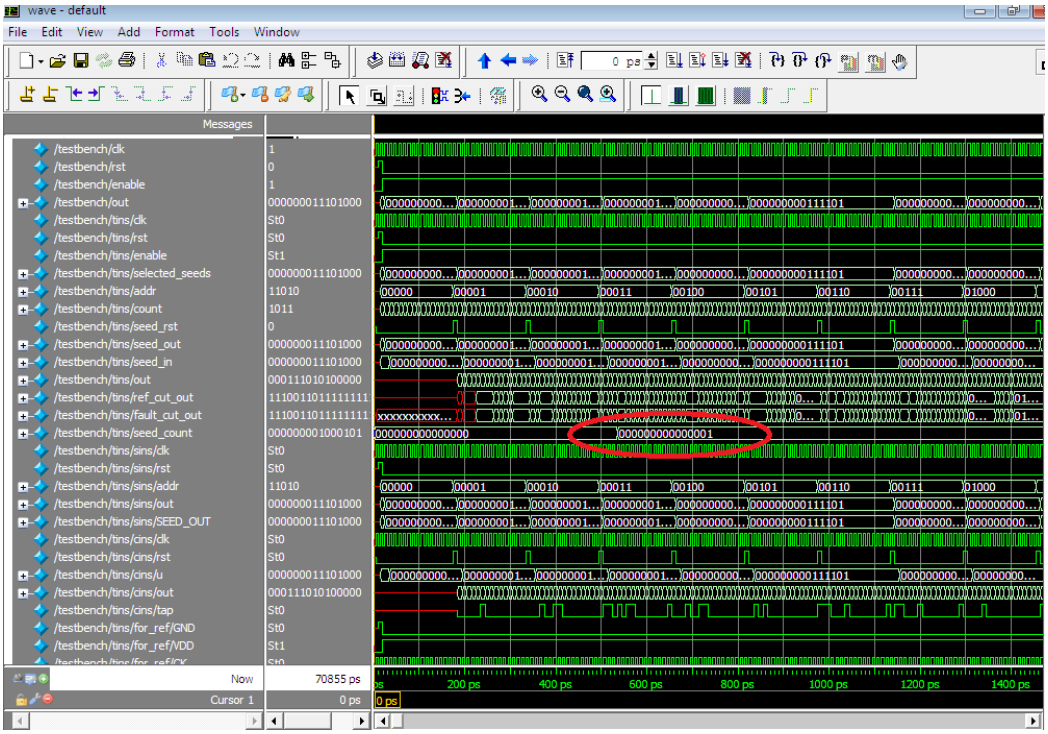

Fig.2. Simulated random output using FSM LFSR TPG

4.2 Hardware synthesis results

In this chapter, we compare the performance metrics of proposed LFSR TPG over conventional reseeding based model and validated the metrics both in terms randomization and complexity trade off measures. The proposed LFSR TPG core is modeled using the Verilog HDL and synthesized using FPGA QUARTUS II EDA synthesizer for state-of-the-art comparison. The resultant TPG as shown in Figure 3 is capable of achieving flexible fault coverage with least possible design complexity and tolerable energy efficiency. Moreover, by exploiting the benefits of reseeding and polynomial computation which can minimize memory space requirements and can able to support the path delay optimization using FSM model. In this memory optimized FSM controller as shown in Figure 4 can able to jointly optimize the computational complexity and energy from beneficiary random TPG computation.

Table 1 Performance comparisons between FSM driven LFSR TPG model using FPGA hardware synthesis results

TPG model	Area(LE's used)	Total Power dissipation(mW)
Conventional LFSR model	34	117.13
Proposed FSM controlled LFSR	65	52.15

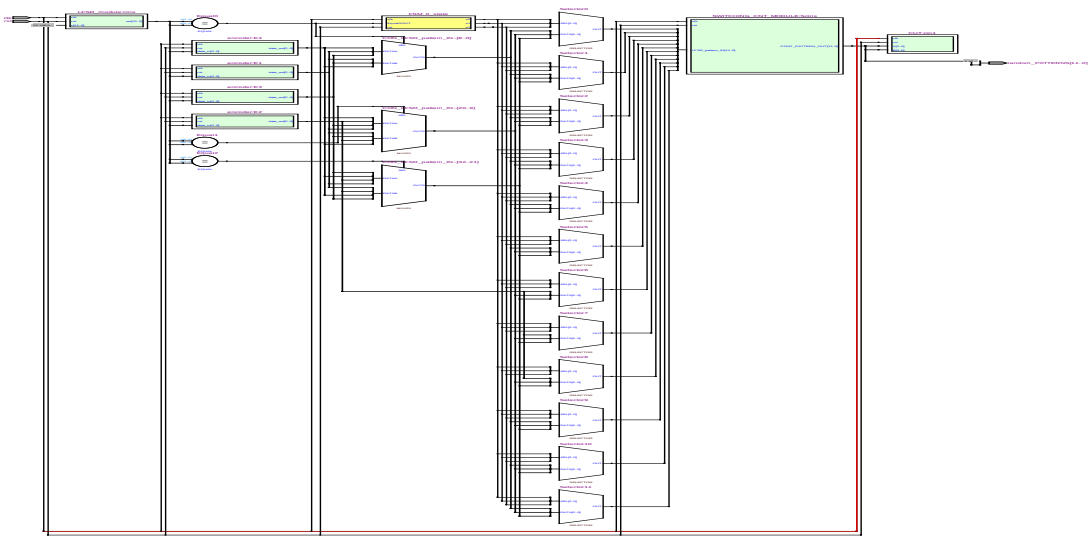

Fig.3. LFSR TPG RTL view

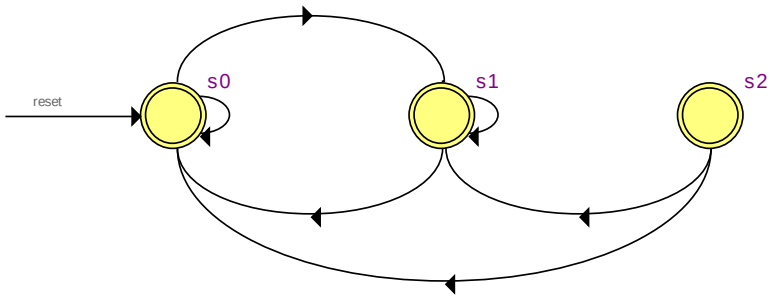

Fig.4. FSM state machine report.

4.3 Performance comparison report

The FPGA hardware synthesizer tool has been used to measure the power utilization report and its experimental results are listed in Table 1. From the logical elements utilization summary it is proved that the proposed FSM based LFSR using variable rate clock model leads significant complexity overhead as compared to the conventional reseeding based LUT approach but offers tolerable energy efficiency. The energy efficiency of memory efficient FSM LFSR is also proved to be the significant one as shown in Figure 5 through FPGA hardware synthesis results.

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Mon Apr 09 13:47:49 2012
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	TOPMODULE
Family	Cyclone
Device	EP1C3T100C6
Power Models	Final
Total Thermal Power Dissipation	52.15 mW
Core Dynamic Thermal Power Dissipation	0.84 mW
Core Static Thermal Power Dissipation	48.00 mW
I/O Thermal Power Dissipation	3.31 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.5. Power dissipation report.

CONCLUSION

Here in this work BIST implementation using modified FSM driven LFSR TPG algorithms is proposed which includes non linear randomization properties. It is also demonstrated that FSM based LFSR introduced for TPG offers potential energy consumption reduction. Here, the investigated multiple instance XOR operations along with random sequence generation model offers BIST scan-protection scheme that provides high fault coverage with least computational time and over the course of the CUTs circuit life. Compared to regular BIST mode, this method is not affecting the fault coverage during testing. Here we proved that FSM based LFSR will give better hardware complexity & power optimization with considerable delay enhancement.

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