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FSM Based Spike Detection for Multichannel Neural Signal Processor

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Abstract: A non-implantable Micro system typically is used to monitor activity of the brain. It requires on-chip real time processor which is processing of multi-channel neural signal with less power consumption and less area utilization. However, it is a challenge to get the less area and minimum consumption of power when the processing of multi-channel neural signal in real-time hardware with spike sorting algorithms. Hence, proposing an efficient neural signal processor (NSP) with optimal design constraints for multi-channel. The Haar discrete wavelet transform (HDWT) algorithm is designed for the NSP to process the spike data detection and sorting of the spikes. The NSP is simulated in Model Simulator 6.4a software and implemented on FPGA target device. The proposed NSP got 3.44ηs of delay and 79.98mw% of power consumption when it is implemented on Cyclone FPGA device.

Keywords: NSP, Spike Detection, Spike Sorting, Multi-channel, Neural Signal.

1. Introduction

The foremost functionality of Central Nervous System (CNS) is to delivery, receive and processing of data from various parts of human body. The brain and spinal cord is associated with CN System. Research area of CNS is classified into two types, one is direct problem in which computer and engineering techniques are involved to observe the human Brain activity. This method is conventionally used by the cognitive scientists in various domains of neurophysiology because the established models are mimics of CNS [1]. Another method is invasive, problem which simulates thereby creating a structure for engineering systems. Based on simulations the basic structures for differential diagnosis and disease process are created with use of inverse problem method. Depending on threshold, the output structure is created with simulated multiple inputs. Advanced Brain Machine Interface (BMI) controls the prosthetic devices in body to record millions of neurons [2]. To eliminate mechanical vulnerabilities and to reduce the infections in prosthetic devices, future generation BMIs should be implantable in neuronal micro system in terms of wireless because systems like this will reduce the heat dissipation and power consumption. The neuron micro system which is included the neural signal processor to avoid the tissue damage by considering only spikes of active neuron and by ignoring the spikes of inactive neurons spikes thereby reducing the neural data [3]. Though reducing of neural data is a critical task, it has to be processed individually to get accurate neuron information by using machine commands. It is known that each microelectrode should observe multiple neurons activities and processed individually.

In real time BMI system it provides the control and general communication into different parts of the body and Nervous system. In addition to this, it also preserving the spikes signals which are generated by brain and these signals are converted into data to control the specific BMI application [4]. The main functionality of BMI system is to record the data which is getting from electrodes as raw information. The raw information can be processed and converted into useful data by different methods to perform particular task by the brain. Once data is recorded, the BMI filters the signal to remove noise and unwanted signals [5]. One of the major techniques in BMI is feature extraction. The feature of denoised data can be extracted by using different analyzers later these spikes are sorted and mapped based on threshold [6]. In this work we are using in built library function in matlab named as *dec2bin()* which is converting decimal to binary. The number of converted binary bits depending up on variable defined in dec2binary function [7].

The proposed work designed and implemented 256 multichannel of neural signal processor. To detect the spikes of neural signal, Haar based discrete wavelet transformation is used and thereafter binary-decision based classified tree is used for classifying and sorting of desired spikes which stores the spike signals in memory through spike ids. FSM based spike detector is used to identify desired spike from classified neural signal.

2. Literature

Daniel Valencia and Amir Alimohammad, designed an efficient hardware for online template matching system for spike sorting. The online template matching system developed and represented based on fixed and floating point system. The developed spike sorting method is used for studying NSP algorithm, recording neural signal information and getting it's amplitude in terms of both online and offline. When it is compared to existing work, online template system presented less power consumption with maintaining high accuracy. However, it presented lower output data rate when compared to existing work because of increase in number of templates in system [8]. Deren Y. Barsakcioglu etl are proposed a behavioral front end model to measure the different parameters such as different types of filter, bandwidth, signal-to-noise ratio and resolution of converter etc,. These parameters are effecting majorly on detection of the spikes and accuracy of the spike sorting. In addition to this, usage of area and power utilizations are also effecting in later stage of spike sorting process. The Analogue front-end based model proposed and validated by applying initial parameters thereby testing hardware circuit with appropriate test stimulus. The response of Analogue front-end based model is as similar as behavioral model when it measured and compared with existing models. This Analogue font based model presented balanced response between resource utilization and performance in terms of accuracy and design time. However, this design decreases the performance of spike processing when compared to existing behavioral models because of decreased resource efficiency [9]Jelena Dragas etc,. are implemented Divide and conquer inspired optimization method for spike sorting which is used to record high density multi electrode arrays. Detected neuron further undergone to the Template matching algorithm. When compare to clustering based spike sorting algorithm, template matching algorithm has advantage of accepting raw data, which is not sorted one. This is algorithm calculates spike templates by averaging the spike signals with reference of threshold values. This algorithm applied into reconfigurable VLSI hardware architecture and hence high performance and low latency presented. The reconfigurable hardware presented optimal bandwidth when compared to previous published algorithms because of it transmits individually with

reference of spike wave forms or spike time stamps [10]. Fei Zhang etc,. are implemented 32 bit neural signal processor for spike sorting and neuronal signal compression. They designed processor based on "on the fly" technique to extract the data from neural signal .The neuro processor implemented on FPGA that dimensions are 5mm x 5mm, it consumes power less than 5mW when sampled neural data at 25KHz with 8 bit data resolution. The proposed system is highly effective in terms of scalability and system cost, hence it is deserved for research on both clinical BMI applications and small animals in neuroscience [11]. G. Gagnon-Turcotte etc,. are implemented optogenetic multi channel wireless head stage to record and stimulation spikes of neural signal. A 32 channel head set is designed with key element namely rigid flex printed circuit board. The head set is a Accurately designed for living animals as it is light weight, small size and easy to handle. It can process 32 real time neural signal channels at a time. By Processing multiple times to collect spikes, the hundreds of data in micro volts spike signal with more signal to noise ratio and higher distortion ratio measured once it is detected and stored in a device [12].

Bonfanti etc,. are used wireless telemetry and data compression techniques consist of to design System on chip(SoC). The SoC is designed to process 64 channel, the internal architecture consist of successive approximation 8 bit analog to digital converter, narrow band 400MHz wireless Frequency shift keying transmitter with 16 amplifiers and analog time division multiplexer. Wireless FSK transmission is used in digital data compression with a rate of 1.25 MBPS stored wave forms and Action potentials. An efficient embedded antenna is designed based on Manchester recorded modulation technique with low frequency, moderate bit rate of stored wave forms. The system on Chip is designed and implemented with 0.35micro meter and 105 micro power watt per single channel. After appropriate verification, the designed system is exhibited two coin battery which is compatible for longer time experiments in neural signal. However, combination of data rate and power is the key for practical use of narrow band RF frequency [13]. Amir M. Sodagar etc,. are designed invasive device for neural recording system to process 64 channel neural signal. it is programmed to identify different spike amplitudes based on logic levels of negative, window thresholding or positive. The identified spike is assigned with 18 bit data of unique number based on it's channel address and hence, sending to the external host serially. The results are monitored and viewed two channels at signal of interest. By adding intra chip modularity feature, the presented architecture compatible for higher recording and higher speed when number of channels are available [14]. In our previous module, we clustered and classified the neuronal spike signals by using matched wavelet transform in wave_clus software [15].

3. Proposed Neural Signal Processor

A. Spike Detection Using Non Liner Energy

Spike events are identified by applying preprocessing and thresholding methods to improve signal to noise ratio (SNR) of the neural signal. As Non Linear Energy (NEO) preprocessing algorithm composed with simple hardware, it is used in huge number of spike detectors [9]. NEO algorithm is used in our work to detect the spikes [16]. Fig.1 shows automatic NEO based spike detector. The mathematical expression for the NEO is expressed in equation 1.

$$\Psi\,(x(n)) = (x\,(n))^2 + x\,(n-1)\,x\,(n+1) \qquad (1)$$

Where Ψ(x(n)) is the NEO coefficient of neural signal x(n).

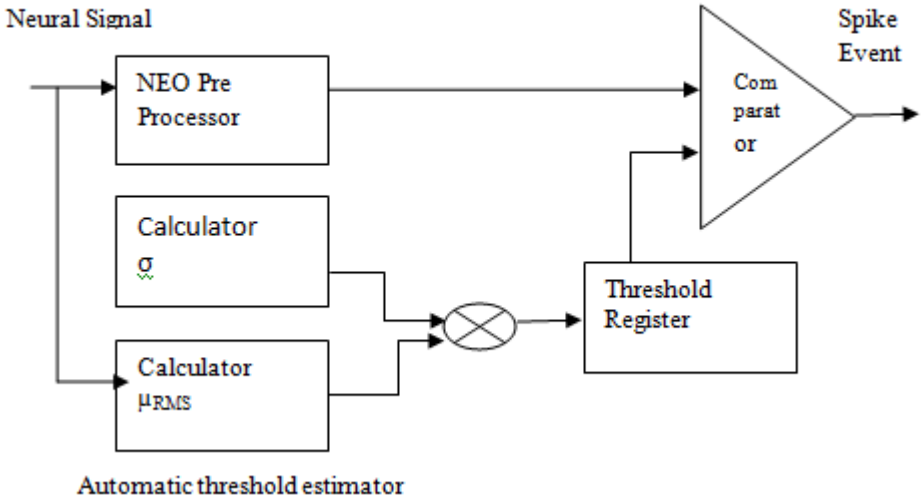

Fig. 1. NEO based automatic Spike detector.

To avoid the drawbacks of conventional threshold technique, our work scaled mean value of NEO coefficient through existing related work. Probability Density Function of unwrinkled noise NEO coefficient E[Ψ(x(n))] and derivational new thresholding method used in proposed work. From literature it is clear that NEO coefficient is not depending on the spike firing rate and it is also flexible to noise level.

B. HAAR DWT

Feature extractor of neural signal is composed with two major blocks those are developed for the purpose of spike sorting that are[17] (a) Haar Discrete wavelet transformation (Haar DWT) based block which stops undesired frequency through filter components [18], (b) peak detector based block extractors the features from detected neural signal. Fig. 2 shows the Haar DWT based feature extractor which is working based on approximation and detailed principal. The output from Haar based DWT block is connected to min and max peak detectors.

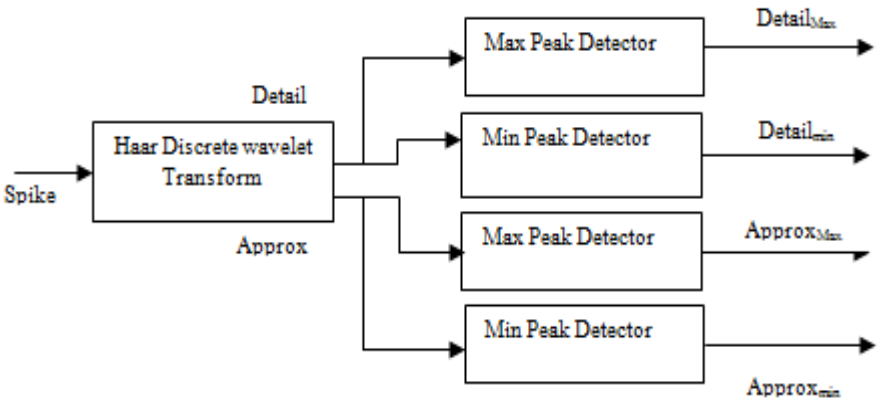

Fig. 2. Haar DWT based feature extraction

C. Automatic Threshold Estimator:-

The noise levels of neural signals are automatically detected by using Automatic threshold spike detectors and varied with respect to the time scale of minutes [19]. The performance Spike detection performance is depending upon the estimator block which is able to track variation of the noise by updating the threshold value within the specified time frame. In our work, Automatic threshold estimator is taking 5 seconds time for single channel to compute a new threshold. Thus, time division multiplexing is using to scale multiple channels [20]. The proposed automatic threshold estimator block utilized 180 seconds of time frame for updating 256 number of channels sequentially.

D. 256 Channel Processing:-

When a spike is detected both the spike classifier and feature extractor are getting active, at the frequency of the spike firing both the blocks are operating and it is much lower than the neural sampling rate. Both blocks are scaled for multichannel processing in same way. These both blocks are idle in most of the same time for single channel and this time is used to detect spikes from the some other channels it's happened for spikes from different channels are not detected at a time [21]. The Spike signal feature extraction and classifier is restricted to Maximum number of channels (Nmax), that points spikes parallel in manner when processing channel Data (Nch). In this case, only Nmax (Nmax < Nch) Feature Extractor & Spike Classifier (FESC) blocks are required for Nch channels. In other words, with Nmax FESC blocks the probability of discarding spikes P rob(Nspk > Nmax) = 0, where Nspk represents the number of channels that fire spikes simultaneously. To reduce hardware cost, a smaller number of FESC blocks, N˜max (N˜max < Nmax), can be chosen such that P rob(Nspk > N˜max) is slightly greater than zero. To study the relationship between Nmax , N˜max and Nch , Nch -channel spike trains of 20 second duration were synthesized using a Poisson firing model at 100 Hz firing rate and the statistic of the number of simultaneously fired spikes (Nspk) across Nch channels was analyzed. When interval between spike occurrence at multiple channels is lower than its spike duration, fired spikes are considered for processing simultaneously.

E. Spike Classifier

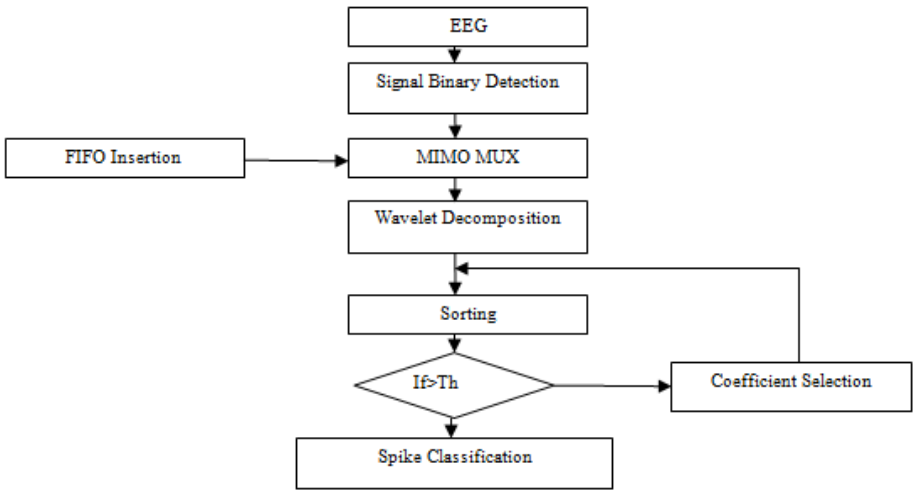

Fig. 3. Spike classification of EEG Signal

Spike classification of EEG is shown in above Fig 3. It is requiring huge memory to store the spikes individually because each spike consists own data and stores in respective channel.Hence, it is a memory inefficient method in high channel count spike sorting [22]. When comparing existing classification methods in terms of mean feature of each cluster, the distance based metric classification is commonly used.

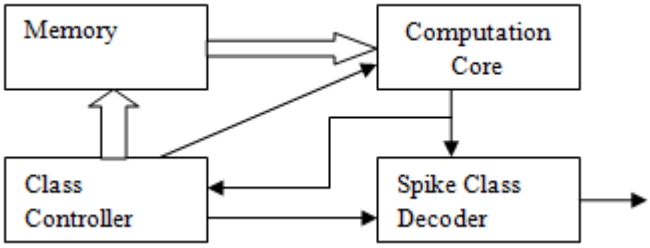

Fig. 4. Binary Decision tree based Classifier

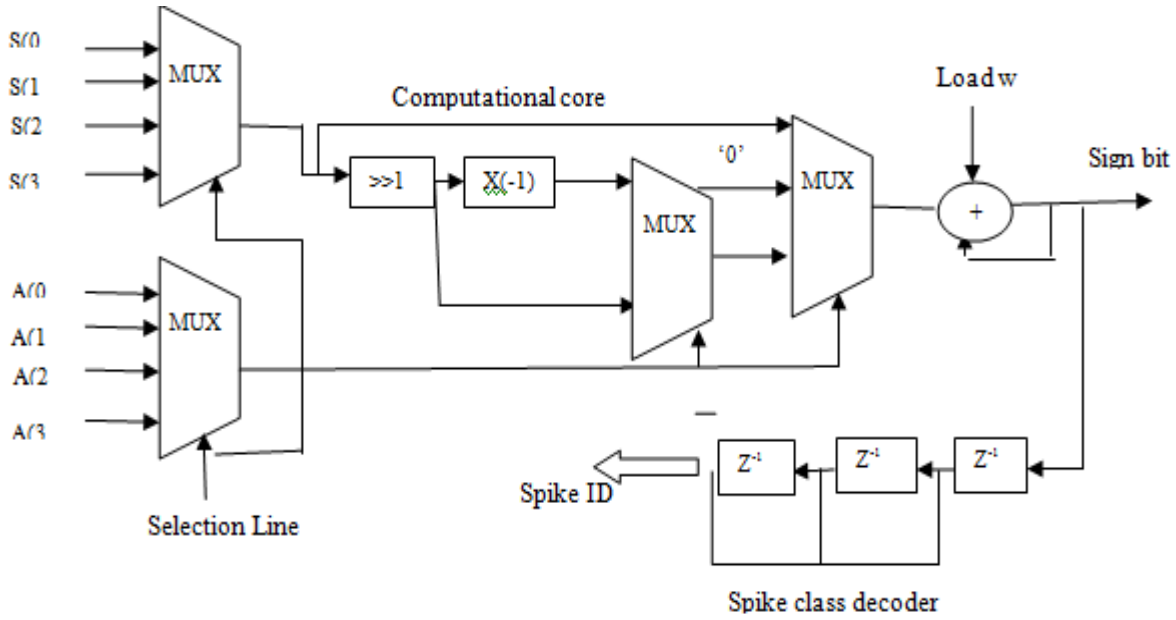

Fig. 5. Spike classification Decoder blocks and computational core schematic.

Conventional distance based methods presented equal weight feature of spikes to differentiate one among them. Though, traditional distance based methods do not contribute distinction of spikes equally, binary decision tree (DT) based method used to identify weights of individual spikes. Fig.4 depicts DT based spike classifier which is designed with controller memory block, computational core and spike class decoder. The computational core process the detected spike based on decision tree node and node coefficient of input spike. After performing of computation core, features of input spike stored at memory block of DT based spike classifier. The controller block receives binary data from the computation core and assigns unique memory address for next coefficient of input spike. The controller identifies finite feature and it's coefficient of spike at every computation core face and hence it transfers spike to decoder module to select output spike ID of child node. Fig.5 explains detailed structure of computation core and also decoder module. The decoder block stores output binary value of each node upto computational core terminates at the child node and

generates unique spike ID from binary decision tree path for the unique sequence. From fig .5, it is clear that the number of neurons recorded at any channel must be less than six and hence spike id is given by three bits.

F. Spike Alignment:-

Spike alignment block requires a reference point of output spike from spike detector and aligns each output spike with reference point. Hence, the reference point of alignment spike plays vital role in further process such as spike sorting [23]. Traditional feature extraction method such as a PCA needs spike alignment block to preserve required samples of neural signal. Features of the spikes can be calculated directly from streaming spike data by using filtering based feature extraction method. In addition to this, reference alignment point does not show any impact on feature extraction or spike sorting [24], because maximum and minimum values of extracted features are considered from filter output. Hence, the spike alignment point is set where detected threshold crossed to minimize hardware cost. The alignment block needs to preserve missing samples as per pre threshold crossing buffer. The performance of spike classification depends on the buffer size and it is described in the result section.

G. Multichannel Implementation:-

A summary of the scalability analysis shows that optimal multi-channel scaling is achieved with a 256-channel NEO Preprocessor and 256-channel Automatic Threshold Estimator, Feature Extractor and Spike Classifier blocks. The design of a spike sorting NSP module can process 256 neural channels simultaneously composed of four NEO Preprocessors. Each NEO preprocessing unit composed with processing interleaved data, one Automatic Threshold Estimator which calculates threshold values sequentially for all channels and 13 FESC blocks that classifies detected spikes from 256 channels. All memory blocks such as Pre-threshold Crossing Buffer, Threshold Register and Classification Memory are linearly extended to 256 channels.

H. FSM Spike Detection:-

Once desired signal is selected from filter section, it is sent to the Finite State machine (FSM) based spike detection section. Fig 6 shows FSM Based spike detection method to identify desired spike from the filter neural signal [25]. At initial stage of FSM, a comparator is used to select a desired signal spike point through reference of threshold. Spike point is identified when data point is greater than six and thereafter 256 data buffered points sent to final stage to identify peak of the spike. Final stage module of FSM utilized 256 clock cycles to identify peaks of positive and negative sides of neural signal.

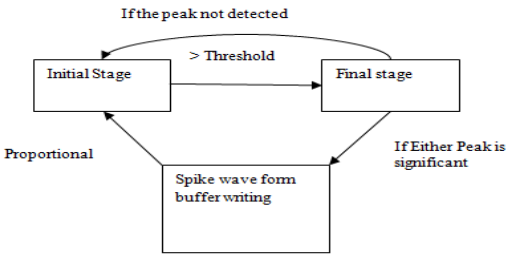

Fig. 6. FSM based spike detector flow chart

If any one of peak spikes is detected, FSM based spike detector moves to the spike wave form buffer module. The buffered state requires 128 clock cycles to write peak into buffer. If peak is not detected, then FSM moves from final stage to initial stage. Once Spike is written into the buffer module, the FSM transferred to initial stage. When desired spike is detected from the FSM, respective spike id and it's time stamp are forwarded to RAM to store it and then detected spike wave form is forwarded to RAM.

4. Implementation

The proposed work is developed in Synthesizable model for FSM based spike detection method. The function of synthesizer is to convert register transfer level (RTL) of FSM based spike detection method into minimized gate level netlist. This is one of the important steps in ASIC which converts RTL model into low level hardware realization. The Synthesis process works in three major steps. "Translation" is the first and foremost step and it converts the RTL logic design into a non-optimized intermediate design through efficient synthesis tool. "Logic Optimization" is the second stage which minimizes the internal representation of design by eliminating redundant logic in design and then optimizing design through Boolean minimization logic. "Technology mapping and optimization" is the last step that maps representations from intermediate to gate level based in built library logic cells of own design constraints. The proposed work is simulated at Modelsim 6.4a simulator and synthesized at QUARTUS-II tool version-9 to present implementation results. The FSM based Spike detector is implemented and analyzed in terms of timing constraints such as operating frequency, delay and also area utilization logic cells and required dedicated logic registers.

Latency measure = 21 clock cycles for channel regulation

52 clock cycles for feature extraction

83 clock cycles for signal classification

Multichannel neural signal is implemented for 256 channels and designed using MATLAB R2014b. Fig 7 shows generation of 256 channels for multichannel and then peak is identified using FSM based spike detector. The channels are taken from the EEG data file from university of Bonn, in the department of epileptology [26].

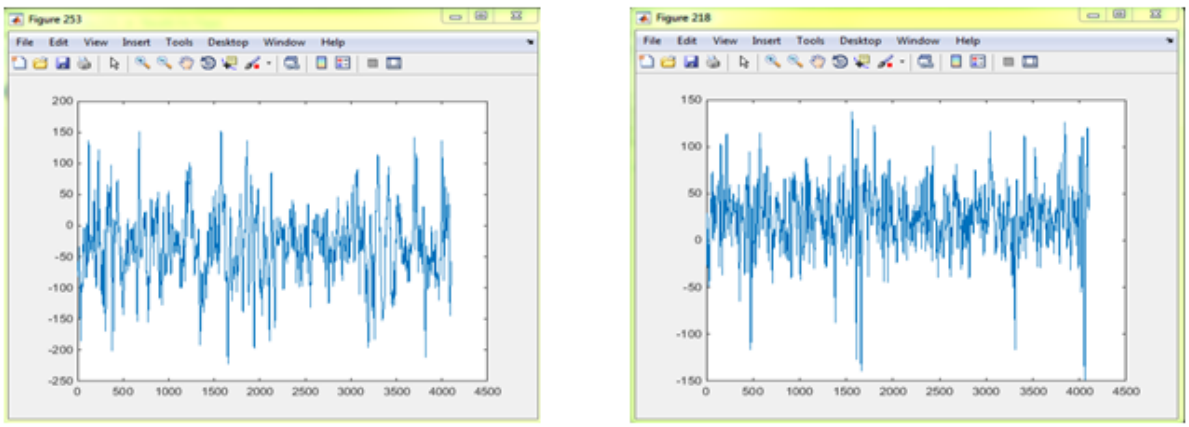

*Fig. 7.*Some Sample images 256 channel MatLab Images

The desired neural signal identified through filter components and applied to neural signal processor. The FSM based spike detector realized at Computer Aided Tool (CAD). Fig a shows output of 256 channel of neural spike signal when simulated at Modelsim. The 256 channel of neural signal are controlled with channel ID and spike ID and output peak spike generated at each channel.

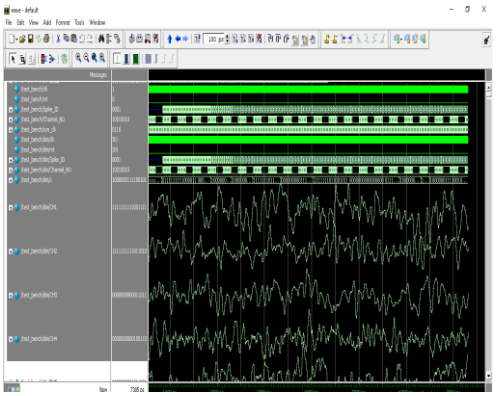

Fig. 8. A Simulated output

Fig.8 presents the area utilization of 256 channels for FSM based spike detection when it is implemented Cyclone-II (EP2C35F672C6) FPGA target device. The area utilization is analyzed with number of logic elements, number of registers and number of pins. From fig. 9, it is clear that the proposed FSM based design utilizes very low area in FPGA when it is prototyped. As design consumes less area overhead, the proposed design is suitable for any advanced hardware to detect spike of neural signal.

Flow Status	Successful - Tue Dec 15 18:04:01 2020
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	NSDTOPMODULE
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	No
Total logic elements	3,165 / 33,216 (10 %)
Total combinational functions	2,956 / 33,216 (9 %)
Dedicated logic registers	1,289 / 33,216 (4 %)
Total registers	1289
Total pins	14 / 475 (3 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Fig. 9 Area utilization report

File Edit View Netlist Constraints Reports Script Tools Window Help

Report

TimeQuest Timing Analyzer Summary
Parallel Compilation
Fmax Summary

Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	INF MHz	81.83 MHz	max_min:MINS1|Buffer10[0]	limit due to hold check
2	INF MHz	93.86 MHz	max_min:MINS2|Buffer10[0]	limit due to hold check
3	38.1 MHz	38.1 MHz	clk	
4	290.53 MHz	155.28 MHz	SELECTION_LINE[0]	limit due to hold check

Fig. 10 Frequency Summary

Fig. 10 shows performance of proposed work in terms of operating frequency. The operating frequency is measured for buffer and selection modules separately as these modules are directly effects performance of FSM based neural spike detector. The maximum utilization frequency of proposed work is 290.53MHz which is compatible for real time hardware which indicates that the delay of proposed work is 3.44 ns.

Throughput is another important metric of proposed work to identify performance of neural signal processor in terms of speed. Throughput is defined as number of data bits transferred at second through desired number nodes. Typically, higher throughput system has proportionally presents higher performance. The proposed work obtained throughput of 4.65 Gbps which is highly suitable for present generation.

Throughput = No. of bits processed per cock cycle x Fmax

= 16 x 290.53x10^6

= 4.65Gbps.

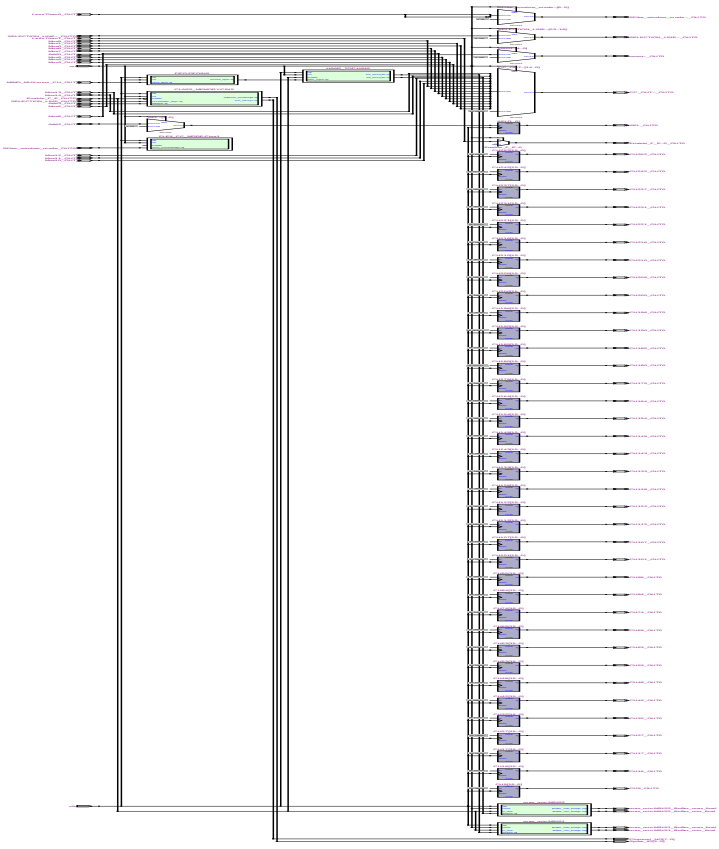

Fig. 11 RTL view of 256 Channel

Fig. 11 shows Register Transfer Level (RTL) structure of 256 channel of proposed neural spike detector. In figure, each block represents individual neural signal with spike detector composed internally. For better quality of figure, some of blocks are shown within 256 neural signals. The controller block selects the neural signal to identify spike from desired portion of filtered section.

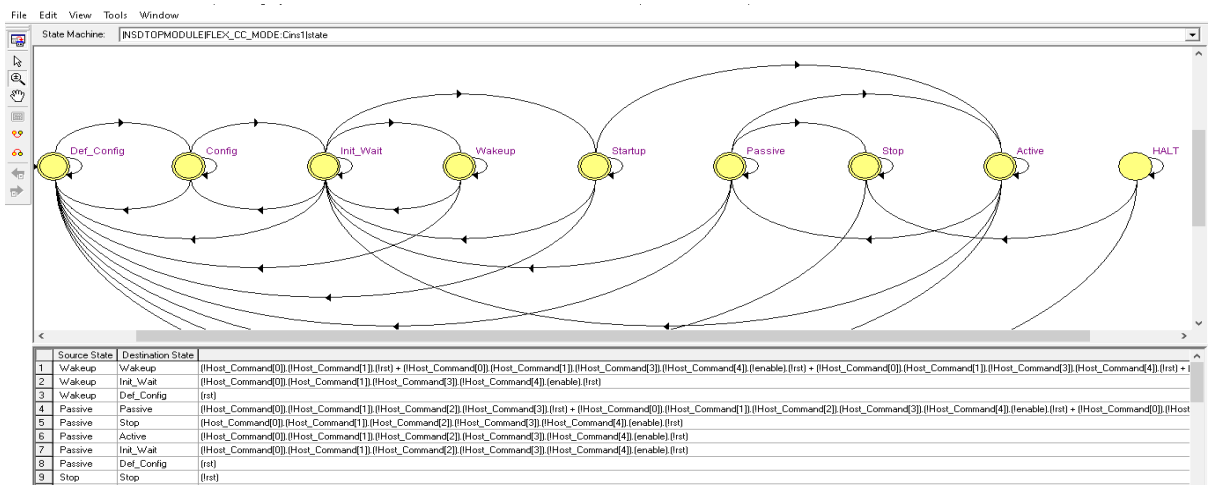

Fig. 12 Schematic of FSM based Spike Detector

Fig. 12 depicts schematic of FSM based model when it is simulated at Modelsim. From structure of FSM based model, it is clear that the peak of spike is detection if state forwards from initial to next state. If peak spike is not detected, then FSM state reverses towards initial state. At the passive state, neural signal waits to detect peak point and forwards to wake up state whenever peak point is detected.

Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	NSDTOPMODULE
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	128.24 mW
Core Dynamic Thermal Power Dissipation	14.63 mW
Core Static Thermal Power Dissipation	79.98 mW
I/O Thermal Power Dissipation	33.62 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig. 13 Power Dissipation Report

Fig. 13 presents power dissipation of FSM based Spike detection method for 256 channels. The power consumption is analyzed with static, dynamic and thermal power dissipation (mW). The total power dissipation for proposed work is 128.24mW when it is implemented at Cyclone-II FPGA target device. For better analysis, the proposed work is implemented with less toggle rate because dynamic power dissipation dominates if toggle rate increases periodically.

Table.1 indicates different modules in FSM based multichannel spike detector, NSDTOP module gives the total information related 256 multichannel Neural Signal processor information in this total number of logic cells (3165) are utilized, dedicated logic register (1289), number of pins (18) and lookup table information(1089). Similarly FLEX_CC_MODE module we implemented the FSM algorithm to detect the 256 spike channels by assigning spike ids, by using Max_min module we are sorting the spikes, MIMO_MUX is used to selecting the channels, DWT_TOP module is implemented to do the spike feature extraction, FIFO module providing the delay and CAM module is designed to calculate the area related to the FSM based 256 channel information all the modules information is clearly provided in the Table 1.

Table 1 Synthesis results of FSM based Multichannel Spike Detector.

Entity	Logic Cells	Dedicated Logic registers	I/O Registers	Memory Bits	M4KS	Pins	LUT Only LC's	Register Only LC's	LUT/ Register LC's
NSDTOP module	3165(62)	1289(29)	0	0	0	18	1876(33)	209(0)	1080(29)
FLEX_CC_MODE	46(46)	12(12)	0(0)	0	0	13	34(34)	0	12(12)
MIMO_MUX	-	0	0	0	0	4120	-	-	-
FIFO	352(352)	297(297)	0(0)	0	0	34	55(55)	112(112)	185(185)
DWT_LEVEL_1	281(0)	195(0)	0(0)	48	1	52	86(0)	0(0)	195(0)
DWT_LEVEL_2	376(0)	269(0)	0	0	0	52	107	46	223(0)
Max_min	750(750)	235(235)	-	-	-	51	515(515)	16(16)	219(219)
Memory Bank	57(57)	9(9)	0	0	0	22	48(48)	3(3)	6(6)
CAM	57/33,216	9/33,216	9	0	0	0	-	-	57/33216
DWT_TOP	1222	737/(33216)	-	-	-	51	-	-	-
HIGH_PASS	658(658)	392(392)	0(0)	0	0	35	266(266)	160(160)	232(232)
HIGH_P	420(420)	222(222)	0(0)	0	0	35	198(1	0	228(2

ASS_1							98)		28)
HIGH_PASS_2	420(420)	222(222)	0(0)	0	0	35	198(198)	0	222(222)
HIGH_PASS_2_1	219(219)	137(137)	0	0	0	35	82(82)	0(0)	137(137)
HIGH_PASS_2_2	219(219)	137(137)	0	0	0	35	82(82)	0(0)	137(137)
LOW PASS	665(665)	399(399)	0	0	0	36	266(266)	160(160)	239(239)
LOW PASS_1	345(345)	229(229)	0	0	0	36	116(116)	80(80)	149(149)
LOW PASS_2	345(345)	229(229)	0	0	0	36	116(116)	80(80)	149(149)
LOW PASS_2_1	156(156)	132(132)	0	0	0	36	24(24)	45(45)	87(87)
LOW PASS_1_1	62(54)	58(53)	0(0)	48	1	36	4(1)	0(0)	58(53)
MUX	35(35)	0/0	0	0	0	106	35(35)	0(0)	0(0)

Table. 2. Comparison of FSM based spike detector with memory efficient spike sorting model.

	Area report			Speed	Power dissipation report	
	Logic cells	Logic registers	LUT's		Static power	Dynamic Power
Memory efficient spike detection model- Existing method[7]	3284	1289	1995	265.67 MHz	80.14mW	63.36mW
NEO spike detection model [22]	-	16245	23567	100MHz	177.92µW	46.08 µW
FSM based Spike detection -proposed method	3165	1289	1876	290.53MHz	79.98mW	14.63mW

Table.2 depicts comparison between memory efficient spike detection model [7] and FSM based spike detection model in terms of area utilization, speed and power dissipation. Both Memory efficient detection model [7] and NEO spike detection model [22] are implemented for 64 channel of neural signal processor, hence the results resented in Table 2 are better than proposed work. However speed of the proposed work is massively higher than both [7] and [22] because proposed

work used 256 channels for spike detection. It is known that number of channels is improves speed of the structure. From Table 2, it clear that proposed method presented higher performance than typical spike detection algorithm. Table 2 inferred that there is very little improvement shown in area utilization whereas speed and power consumption improved considerably because FSM of proposed design advances the detection speed of peak spike. From previous work [15] and above results, the latency and area overhead are decreased when proposed work implemented in FPGA. Hence, the objective of minimizing latency and area overhead is fulfilled with implementation results of spike detection and wavelet transform based clustering.

5. Conclusion:-

In our work we designed multichannel FSM based spike detection unit for 256 channels, these input channels are initially processed in MAT Lab R2014b. Our system multichannel spike detector is implemented on Cyclone FGA device it consuming 79.98mw% power and 3.44ηs delay. Compare to the existing system, our system consuming lesser power dissipation and higher speed. The proposed work directs to detect seizer disease and to identify epilepsy based on storing of spike ids in memory unit. In our feature work, the performance of neural signal processor evaluated using FIFO and FSM based scheduling algorithm.

References (APA)

[1]. Erhardt, J. B., Fuhrer, E., Gruschke, O. G., Leupold, J., Wapler, M. C., Hennig, J., ... & Korvink, J. G. (2018). Should patients with brain implants undergo MRI?. *Journal of neural engineering*, *15*(4), 041002.

[2]. Ghane, P. (2015). *Silent speech recognition in EEG-based Brain Computer Interface*. Purdue University.

[3]. Darmanjian, S., Cieslewski, G., Morrison, S., Dang, B., Gugel, K., & Principe, J. (2006, January). A reconfigurable neural signal processor (NSP) for brain machine interfaces. In *2006 International Conference of the IEEE Engineering in Medicine and Biology Society* (pp. 2502-2505). IEEE.

[4]. Vanga, K. R., & Kumar, A. V. (2019). A Review on Recording of Neural Signal to Monitor Brain Activity. *International Journal of Advanced Studies of Scientific Research, Forthcoming*.

[5]. Wang, Y., Zeng, H., Song, A., Xu, B., Li, H., Zhu, L., ... & Liu, J. (2017, May). Robotic arm control using hybrid brain-machine interface and augmented reality feedback. In *2017 8th International IEEE/EMBS Conference on Neural Engineering (NER)* (pp. 411-414). IEEE.

[6]. Yang, Y. (2016). *A hardware-efficient VLSI neural signal processor for implantable high-channel-count brain machine interfaces*. Michigan State University.

[7]. Yang, Y., Boling, S., & Mason, A. J. (2017). A hardware-efficient scalable spike sorting neural signal processor module for implantable high-channel-count brain machine interfaces. *IEEE transactions on biomedical circuits and systems*, *11*(4), 743-754.

[8]. Valencia, D., & Alimohammad, A. (2019). An efficient hardware architecture for template matching-based spike sorting. *IEEE transactions on biomedical circuits and systems*, *13*(3), 481-492.

[9]. Barsakcioglu, D. Y., Liu, Y., Bhunjun, P., Navajas, J., Eftekhar, A., Jackson, A., ... & Constandinou, T. G. (2014). An analogue front-end model for developing neural spike sorting systems. *IEEE transactions on biomedical circuits and systems*, *8*(2), 216-227.

[10]. Dragas, J., Jäckel, D., Hierlemann, A., & Franke, F. (2014). Complexity optimization and high-throughput low-latency hardware implementation of a multi-electrode spike-sorting algorithm. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, *23*(2), 149-158.

[11]. Zhang, F., Aghagolzadeh, M., & Oweiss, K. (2011, May). A low-power implantable neuroprocessor on nano-FPGA for Brain Machine interface applications. In *2011 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)* (pp. 1593-1596). IEEE.

[12]. Gagnon-Turcotte, G., LeChasseur, Y., Bories, C., De Koninck, Y., & Gosselin, B. (2015, October). A wireless optogenetic headstage with multichannel neural signal compression. In *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)* (pp. 1-4). IEEE.

[13]. Bonfanti, A., Ceravolo, M., Zambra, G., Gusmeroli, R., Spinelli, A. S., Lacaita, A. L., ... & Fadiga, L. (2010, September). A multi-channel low-power system-on-chip for single-unit recording and narrowband wireless transmission of neural signal. In *2010 Annual International Conference of the IEEE Engineering in Medicine and Biology* (pp. 1555-1560). IEEE.

[14]. Sodagar, A. M., Wise, K. D., & Najafi, K. (2007). A fully integrated mixed-signal neural processor for implantable multichannel cortical recording. *IEEE Transactions on Biomedical Engineering*, *54*(6), 1075-1088.

[15]. Vanga Karunakar Reddy., Dr Ravi Kumar AV. (Oct-Dec' 2020).OPTIMAL CLUSTERING TECHNIQUE FOR NEURAL SPIKE SIGNALS WITH MATCHED WAVELET TRANSFORM. International Journal of Interdisciplinary Global Studies ISSN No: 2324-755X Volume: 14, Issue No: 04,Oct-Dec' 2020 (pp. 115-119).

[16]. Zeinolabedin, S. M. A., Do, A. T., Jeon, D., Sylvester, D., & Kim, T. T. H. (2016, June). A 128-channel spike sorting processor featuring 0.175 μW and 0.0033 mm 2 per channel in 65-nm CMOS. In *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)* (pp. 1-2). IEEE.

[17]. Valencia, D., & Alimohammad, A. (2019). A real-time spike sorting system using parallel OSort clustering. *IEEE transactions on biomedical circuits and systems*, *13*(6), 1700-1713.

[18]. Shaeri, M. A., Sodagar, A. M., & Abrishami-Moghaddam, H. (2011, September). A 64-channel neural signal processor/compressor based on Haar wavelet transform. In *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society* (pp. 6409-6412). IEEE.

[19]. Ramacher, U., Beichter, J., Bruls, N., & Sicheneder, E. (1993, May). Architecture and VLSI design of a VLSI neural signal processor. In *1993 IEEE International Symposium on Circuits and Systems* (pp. 1975-1978). IEEE.

[20]. Qian, C., Shi, J., Parramon, J., & Sánchez-Sinencio, E. (2013). A low-power configurable neural recording system for epileptic seizure detection. *IEEE transactions on biomedical circuits and systems*, *7*(4), 499-512.

[21]. Moustafa, A. A. (Ed.). (2017). *Computational models of brain and behavior*. John Wiley & Sons.

[22]. Gibson, S., Judy, J. W., & Marković, D. (2013). An FPGA-based platform for accelerated offline spike sorting. *Journal of neuroscience methods*, *215*(1), 1-11.

[23]. Valencia, D., & Alimohammad, A. (2019). A real-time spike sorting system using parallel OSort clustering. *IEEE transactions on biomedical circuits and systems*, *13*(6), 1700-1713.

[24]. Xiong, T., Zhang, J., Martinez-Rubio, C., Thakur, C. S., Eskandar, E. N., Chin, S. P., ... & Tran, T. D. (2018). An unsupervised compressed sensing algorithm for multi-channel neural recording and spike sorting. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, *26*(6), 1121-1130.

[25]. Liu, Y., Sheng, J., & Herbordt, M. C. (2016, September). A hardware design for in-brain neural spike sorting. In *2016 IEEE High Performance Extreme Computing Conference (HPEC)* (pp. 1-6). IEEE.

[26]. Phys. Rev. E, 64, 061907.