Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 8, July 2021:1945 - 1957

Implementation Of ECG Signal Compression by Using FFT System

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ABSTRACT

This report presents an SPIHT encoding method electronic cardiovascular device. The low-performance architecture equipment is intended to implement a high-performance, cheap ECG in real time. SPIHT uses more sophisticated coding, which uses the modified wavelet's characteristics to enhance its effectiveness. Consequently, current SPIHT systems have been built to handle photos and recordings. Such systems need a lot of memory and are complex repetitive and unsuitable calculations for mobile ECG. Banners and scan bits have been improved to reduce story needs and to encode impredictability by combining three formats at one level, given the latest advancements in our spith coding functionality. Therefore, we provide in this article a translator assessment for SPIHT-situated devices suitable for decrypting the newly chosen SPIHT encoding function to accomplish the continuing program goal of mobile applications of ECG. Digital signal processing (DSP) computation is used as frequently as feasible for the usage of orthogonal frequency multiplexing. The quick fourier transform (FFT) transform (OFDM). The combination of Multiplexing Orthogonal Frequence Division (OFDM) and Multiple Multi-Input Output (MIMO) handling is a clear means to upgrade the information rates of various mailing frames, such as Wireless LAN, eMobile, 4G, and so on. Since FFT is a complex module inside OFDM, a productive design for the processor is very inevitable. This study included the use of low-delay and area-efficient frequency and time radix-2 (DFT) decimation by radix-2 butterfly.

Keywords: *ECG, Spihtdecoder, Mobile Health, FFT, DFT.*

INTRODUCTION

Scientific management of data signs in order to adapt or improve the digital signal processing (DSP). It is represented by a series of numbers or pictures representing discreet time, discrete recurrence, and other discrete zone signals and preparing such signs [1]. DSP aims mainly to non-stop authentic, simple signals, channels and/or parcels. The first stage is mostly to alter via the sign, by checking and digitizing it by a basic to-computerized converter (ADC) which converts the simple sign into a range of numbers. However,

the necessary rating sign is usually another basic rendering signal, which needs an advanced to a simple converter (DAC). While the use of computer energy is more strange than simply preparing, it has a different range of values. In many applications, for instance misidentification and revision of transmission and extra information pressure are of great concern in the use of advanced sign handling computer energy. DSP computations have operated on ordinary PCs for a while and, furthermore, on special processors, such as application particular coordinated circuit termed advanced sign processor and intentionally built equipment (ASICs). Additional advances have been used today in the production of computerized signals, including more intensely-based, generally useful chips, field programmable gate arrays (FPGAs), advanced sign controllers (usually for mechanical applications, such as engine control systems), and stream processors, among others [2-3]. The FFT is among the sophisticated preparation calculations most often used. From now on, the MIMO-OFDM correspondence frameworks were usually used as part of sophisticated sign handling linked for OFDM.. FFT/IFFT processors are important segments to a distant IEEE 802.16 broadband correspondence framework based on orthogonal recurrence division (OFDM); it is one of the most unexpected and focused calculation units for the various physical layer from remote guidelines (ofdm802.11a, MIMO-OFDM 802.11, 802.16,802.16e) [4]. For the RFFT computation, several collapsed pipeline models were suggested[4] that are multiplied into little rational unit butterfly operations. [3]. The [3] and [4] structures may offer certain applications successful performance but the ability of those structures to be diversified continues to be high. In addition, a few of RFFT structures with specific pressing computations were proposed[5],[6]. » A major test in computational outlining and structures for computational calculation is seen as Memory-struggle for read/compose operation[7]. As of late, the idea of continuous preparation of RFFT was to develop a free engineering and strife-free memory to conspire [8]. The FFT computations are classified into two broad types, namely the in-time decimation (DIT) and the in-frequency decimation (DIF) calculations. The main difference of both is seen in Fig. 1. If DIF calculations occur (Fig. 1(a)), in its normal request the information tests are strengthened to the registration structure, while the return is produced in bit changed request. If DIT computation occurs (fig. 1(b)) again, then the information tests must be re-ordered by bit-inverse before being dealt with, while the FFT rates are generated on a typical request. The whole info-gruppen is in the most part available for the FFT computation in different RFFT applications, such as image and video processing, biological sign preparation, time-order surveys, etc. For such applications, DIT RFFT offers an advantage over DIF, because the DIT RFFT structure does not have to wait for the entry of the input samples, but may generate the output once they are calculated.

LITERATURE REVIEW

Pramod Kumar Meher et al.[7] The Fast Fourier Transform pulverization (FFT) has a common benefits over the in-repeat FFT annihilation for most of the certified applications, such as talk, pictorial/video handling, biological signage preparation and time game plan testing, etc.. The butterfly from DIT FFT is also less estimated than its partner from DIF. In this article we present a workable structure for the FFT certified for radix-2 DIT (RFFT). Here, we show the basic numerical listing to remove redundancies from Radix-2 DIT RFFT and offer a definition to regularize its stream charts to permit the drop estimate by means of a direct control unit. We are proposing an enlist-based limit chart, which essentially includes fewer areas to the disadvantage of the relatively higher differentiated dormancy and the traditional RAM. DIT RFFT estimate with enrolment-based limit takes a step forward in the following reading processes as well as creating activities in the same time-cycle in various areas. Therefore, for the suggested DIT RFFT structure, we are showing here a direct meaning of area time. In terms of size, FFTs 16, 32, 64 and 128 are

all included in the suggested design which include 61% less space and 40% less power use than the ones contained in[8]. It contains 70% less postponement of the zone and 57% more of the imperiality of each sample for the comparable FFT sizes as those of another.

This short offers Manohar Ayinala et al.[8] a new adaptable structure for setting up snapshot change of Fourier (IFFT) for actual looked at indications. A modified radio-2 calculation eliminates excess jobs from the stream diagram is used to produce the suggested figure. There are two Radix 2 butterflies that are capable of making four parallel contributions for a second deal with segment (PE). An epic, conflict-free memory architecture aims at ensuring the FFT processor's continuous job. In addition, the design tends to strengthen many parallel PEs. In the meanwhile, the suggested actual FFT processor needs fewer estimates and reduced hardware costs look differently from previous studies. In a 256-point certifiable speed of change Fourier (RFFT), the suggested Framework with the 2 PEs reduces the figuring cycles by the 2 segment, while maintaining a lower gear unusuality. With the expansion in the number of PEs the quantity of estimate cycles is decreased.

Shashank Mittal et al.[9], Fast Fourier Transform (FFT) is a leading and most important Software-Defined Radio operation (SDR). Therefore, it is crucial to outline a broad, changeable FFT block with low range, postponement and monitoring requirements. Since late it has been shown that Bruun's FFT is in the ideal world for SDR even with greater part accuracy to maintain the same NSR. This article proposes another engineering process to use Bruun's FFT to increase the bit amount (exactitude) using successive phases of FFT. The suggested engineering also shows that the requirements of the Bruun FFT with intangible modifications in its NSR are further reduced. Bruun's FFT, a better option in SDR for most practical situations, is the outline presented. A point-by-point correlation is performed with Bruun's usual and planned equipment configurations for the same NSR, including the impacts of FPGA and ASIC use.

Byung G. Jo et al. [10] offers a new fast Fourier changing (FFT) processor using an MR calculation (radix -4/2) and a new set-up method, a persistent radix mixed stream (CFMR). The present configuration process supports only an established radix FFT computation. The suggested setup may, of course, reinforce the MR calculation allowing CF FFT computations which pay little attention to the duration of FFT. This epic placement method is carried out by swapping butterfly yield storage regions. MR calculation, the set-up system, and the CFFT computations are provided in the meanwhile by the CFMR FFT processor. Because of the suggested method, the CFMR FFT processor needs just two word memories. Moreover, it uses one butterfly unit that may produce one or two radix-4 butterflies. The 0,18m SEC cell library processor CFMR FFT has 37,000 door recesses, needs only 640 clock cycles for 512-point FFT and is 100 MHz. The CFMR FFT processor may thus decrease the multi-faceted character of equipment, as well as contrasting calculation cycles, and current FFT processors.

EXISTING SYSTEM:

Existing One Dimensional Wavelet Based Quality Assured ECG

The current SFPIHT-producing and equipment-satisfied coding system [12] has been introduced, not at all, in the same way as the earlier systems of SFPIHT using a standard list-based SPIHT measurement [12] as shown in the figure. The SPIHT system has been added to this. 1. The results demonstrate the great efficiency and low power of VLSI. 1. In Figure 1.1 all three squares, DWT and lossless SPIHT functions are on the encoder side (listed as violet). In the interim, a lossless coding scheme SPIHT must be implemented with[12] and SPIHT is represented in the related Nitty Grainy software. The SPIHT lossless

input C[n] is first sorted using the 1-D n-point DWT coefficients and then allocated to a bit plane using the C[n] coefficients. In the bit planes, the quantified coefficients C[n] may be subdivided into two parts: the sign section, S[n] and the scale section.

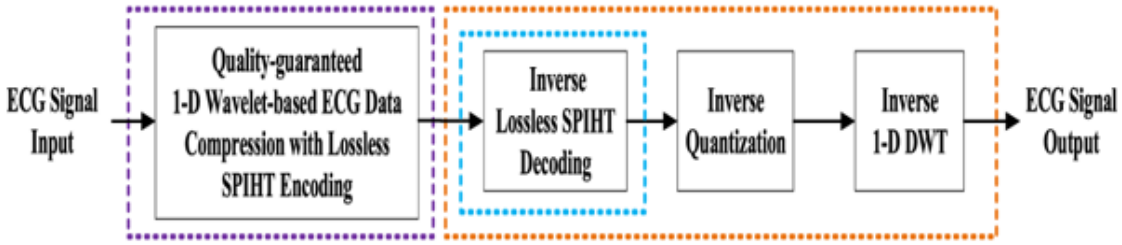

Figure 1: Wavelet Based Quality assured ECG Compression System

The [6] design software offers the respective CCBF and CSF, two types of well-disposed machine registry documents. The CCBF verifies the big coefficients in the layer bit planes. If a big propeller exists, which in contrast to the CCBF area is legally tiny (i.e. '0'), the powerful, stable standard (i.e. "1") will be maintained. On the other hand, CSF records the coding state of each layer hub. If a status indicates a highly flat center, the comparative CSF is therefore configured to be consistently high; normally the default is significantly weak. The sorters (i.e. TACCBF & TACSF) and the forms (i.e TBCCCBF and TBCSF) of 1-D N via 1 DWT implementation may also be categorised as 2 kinds of recorded materials. The specified type A data is utilized for logging of the descendants coefficients of any core layer in the bitplane and is about 2⁄2 bits in scale of each record. Type B register database series are frequently used to register the respective coefficients on the bit plane in each layer coding center and need about 4 bits. All register forms are then arranged in the same way that other N-bit registries (SCSF) are used to monitor the indications of the layer center on the bit ground. Ultimately, the final [n] part is used in each BL [n] layer coding result and a fast 1-D SPIHT coding set-up may be implemented. Thus, this type of codeing comprises the SPIHT's coding computations (11 = to-N / to-dwt) and a bit-planner (11 = to-N / to-dwt) for 1-D N / to-1. The register usage calculation is much higher than the strongest tructures in the class SPIHT[2, 11, 12][6]. Of the strongest techniques in the SPIHT class,[12] only requires to report data from each encoding layer and to alter the encoding condition to improve equipment engineering parallelism so that codes are greatly maximized. In contrast, data from each layer must only be encoded using the method in [12].

SPIHT DECODER ALGORITHM

Stage 1. The core meaning may be described as the difference between the systems of generalized interpretation, which encompasses two types of interpretation. The coding status of SCSF, TACSF, and TBCSF is one focus of the CSIP. Even though the N-bit and the (N/4)-bit are TBCSF (N⁄2) bit and (N/4) bit files, as illustrated in Fig. 2, they are both TACSF and SCSF banner files. In the case of SCSF, TACSF, and TBCSF, all of the parameters are identical. "N⁄2" disengages while "0" and "N/2" remain in place" (0). While the status log from SCSF (N) to SCSF (0) is used to signal whether the decoded hub sign-piece has been established, the sign-coding status log from SCSF (N) to SCSF (0) is also used to flag the hub sign-piece decoding as either valid or invalid. Bit plane threshold FT(L)=2log2(max[croot])-L is used for delegating the layer to the l-th.

- Step 2) Subsequently, CSBSDP processes and updates the current decoded side of recent coding status data for the SCSF, TACSF and TBCSF code status. In contrast, the information O[L] bitstream is finally decoded into the S[N] signage and the material ML[N] scale. Similarly, yield any sub-layer that matched the current RL[N]-th- bit stream decoded soon afterwards, uncoated with a 2 root {ML[0], SF(0), ML[1], SF[1]} structure. If both S[N] and SCSF[N] have the same signal power independently, SF(N) equals S[N]. The return must not be sign outcomes, another element.
- THE Stage 3) The penultimate breakdown is LDOP, which handles the final output of the unreleasedC[N] bit stream. The last stage 2 will be repeated until the FT (L) reaches 0, indicating that the separation phase is complete. The average square graph of our implementation structure, including the 4 encoding units of CSIU, the bit-plan estimating unit (BPTCU), CSBSDU and loss-free analytical output unit (LDOU), is shown at this time in surface Figure.2. Figure.1. In the previous part, CSIU and BPTCU are utilized to illustrate the potential of Phase 1. The CSBSDU and the LDOU are now utilized independently to comprehend the components of previous stages 2 and 3.
    - Step 4) As followed, we describe our proposed SPIHT decoder design system particular methods. Next, O[L] information from the yield of the SPIHT encoder is collected in the translation square and sent correctly to the BPTCU. We designate the CSIU to take the plan balance into account in a particular preparation procedure. The BPTCU and the CSIUs should be utilized to identify each translation layer limit and to individually introduce coding status documents SCSF, TACSF and TBCSF The status documents and the bitstream LTH sub-layer of the Software Development will subsequently be sent to CSBSDU. Application Dec is applied to the reading theory in the CSBSDU to get the total.

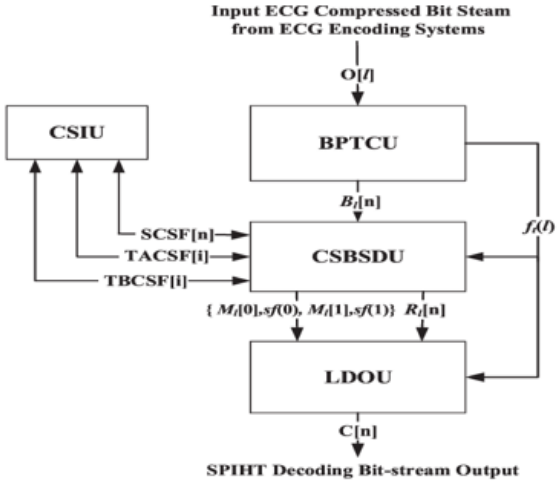

Figure 2: Block Diagram of Our Proposed SPIHT Decoder Design

LTH transforms the sub-layer of the bit stream and modifies 3 coding status records. In combination with numerous coefficients and shifters, CSBSDU system performance is only 1 state-restricted (FSM) freezer. For the LDOU which stores two short root data {ML[0],SF(0),ML[1],SF(1)}, and an input reference

bitstream {N]} in the internal processor with a length of 1.38 kB and provides the last unlike C[N] bits. The dissimulation bit stream is basically sequential.

SPIHT ENCODER

- We propose a highly scalable image compression technique based on the hierarchical trees (SPIHT) method. Our highly scalable SPIHT (HS-SPIHT) method incorporates scalability in spatial and SNR formats and provides a bit stream that is adapted to meet bandwidth and resolution constraints with a fast transcode (parser). The HS-SPIHT method provides a scaling feature without losing the inherent ness characteristic present on the original SPIHT bit stream. HS SPIHT has gradual VHDL applications introduced in XILINX ISE 14.5 (VHSIC hardware description language).
- · The processing and wireless data broadcasting is one of the major difficulties to enable multimedia mobile data services. With further improved bandwidth expected in the future by the wireless access technology, advances in the battery technology will postpone future rapidly increasing energy needs of wireless data services. One way to mitigate this significant problem is to reduce the amount of multimedia data sent via wireless channel compression techniques. An important inspiration was found in the work carried on on MDC techniques like as JPEG[1,2], JPEG 2000[2] and MPEG[3]. Both techniques are based on an increase in the pressure ratio without affecting the efficiency of images. However, such methods will ignore the use of compression and RF energy transmission.
- • Today hospitals utilize their medical image information by means of a machine. Computers and a network enable the transmission of image data to workers efficiently. Modern technologies and techniques such as MR and CT processes are created thanks to computerization in healthcare[4]. MR and CT make an intersectional photographic series (image stacks).
- There is a great deal of information generated by these methods and it may be difficult to transfer the data across a network. To resolve this graph, this data may be compacted. For T-wo-dimensional data, compression methods such the JPEG, GIF, and the newest JPEG2000 wavelet-based formats are available [7]. The following methods are employed with two-dimensional (photo) data, which may not be perfect to compress three-dimensional information such as picture packs, while great for the photographs.

DISCREATEWAVELETTRANSFORM

Computing wavelet coefficients at all conceivable scales is quite a task and gives many details. The manipulative wavelet transformation is equally as powerful and precise if two forces – the so-called dyadic scale and position – are used to choose indicators and lead roles. It is achieved using a discreet wavelet for transformation (DWT).

PROPOSED SYSTEM:

In relation to Radix16 butterfly-based architecture, the memory-based architecture is chosen. This part of the design changes and improves the conventional architecture in order to allow fast DFT (DFT computation) with little hardware requirements. According to Fig. 2, the proposed FFT processor consists

of the following components: 1) Ping Pong data memory, which consists of two memory groups that are each capable of storing 16-bit data as well as a 14-bit image (28-bit data placenta including the real part of a 14-bit frame, and the pixel part of an image of a 14-bit frame); 2) a BFP [5] memory for storing BFP coefficients; and 3) TF multiplication is performed on the CORDIC unit. The alignment unit and the scaling unit implement the harmonization operation and the scaling operation correspondingly for BFP activities.

FFT PROCESSORS

The quickest Fourier transform and Fourier transform are the fastest and most efficient Fourier transform and fourier transform computer techniques. Transformation/investment in Fast Fourier In many communication applications, Fourier Transform is primarily used, for example digital signalling. During the last few years OFDM has become important and is being utilized in FFT procedures. The efficient multi-access technology is OFDM in digital communication (Engels, 2002; Nee & Prasad, 2000). Several of today's OFDM methods may be utilized in the leading wireless communication systems: Digital Audio Broadcasting (DAB) (World DAB Forum, n.d.), Wireless and digital video broadcasters (DVB) (MB- OFDMUWB). This method is also being used in more important wireless applications such as Asymmetric Digital Subscriber Line (ADSL) (PLC). In any communications system, both the transmitter and the recipient must be.

IFFT is utilized on the side of the transmitter for signal modulation, depending on the system OFD, while FFT is used on the receptor side for signal desmodulation. The FFT/IFFT is the main modules in ODFM transceivers. For this reason, IFFT may be used as a viterbi decoder on the receiver side of the transmitter, like the majority of OFDM systems (Maharatna et al., 2004). FFT is the recipient's second large part of calculations. Consequently, FFT and IFFT implementation should be created to provide the required throughput with a reduced area and latency. The demanding conditions of modern OFDM transceivers occasionally result in the installation of specialist hardware in the most critical areas of the receiver. The FFT/IFFT system is thus ubiquitous, utilized as a high scale integrated (VLSI) circuit. The FFT techniques may also be utilized in the IFFT. Furthermore, it is possible to manipulate the FFT processor output via IFFT easily. The FFT without losing its generality will thus be focused on this chapter. Fourier may be found the reverse, discreet transformation In which the twiddled approach is termed What can be stated The difference between Fourier's discreet reverse and Fourier's reverse is a twiddled factor and the 1/N division is called a twodown factor.

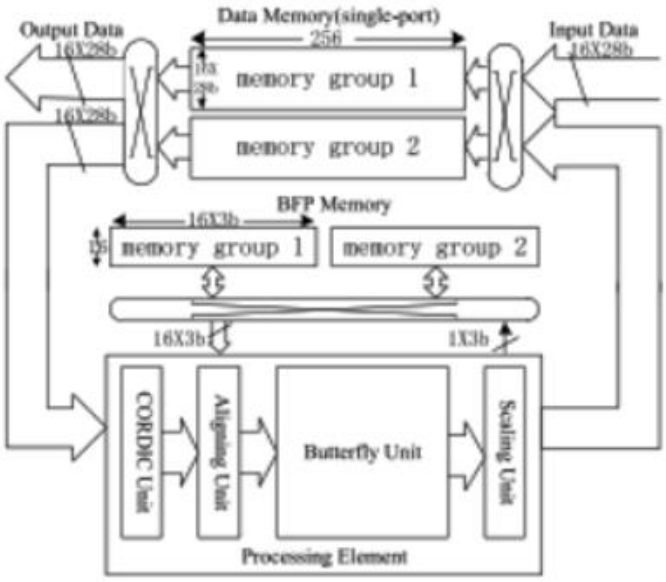

FIG. 2. STRUCTURE OF THE PROPOSED FFT PROCESSOR (ADDRESSING IS HIDDEN).

Various inputs Multiple output systems (MIMO) are wireless communication systems utilized. Multiple output systems. These devices are composed of sends and recipients. High data may be obtained with the MIMO device. Thus the MIMO-OFDM system combination ensures effective wireless communication data speed and dependability. A wireless communications standard (WIMAX) for IEEE 802.16 (Worldwide Interoperability for Microwave Access) may offer data speeds of 30 to 40 megabits per second. The recently evaluated IEEE 802.16 WiMAX 3GP (3rd Generation Partnership Project). 3GPP. A Strategic Partnership effort developed between Northern and AT&T Wireless networks. The third generation partnership project idea In 1998 in the United States AT&T Wireless operated a wireless IS-136 (TDMA) network. To decrease the runtime memory by utilizing a method of memory programming, 12 memory blocks are required instead of 16, RAM is converted into DRAM. The wireless section of Bell Northern Research, an R&D facility in Richardson (Texas), has created a concept for a wireless network with an internal term "cell web" for a "All Internet Protocol (IP)" network. The ram is replaced with a dynamic ram in the suggested architecture.

Butterfly Unit:

Several butterfly units to sustain different radicals have been proposed. The reuse of hardware adders and multipliers by a butterfly unit supports butterfly operations for radix-2, -3, -4, -5 and -7. The enhanced delaying element matrix in [15] allows the 2-D DFT processing method of butterfly processes in radix-2, -3 -4, -5, -8, -9, -16 and -25. The small butterfly high radius unit in [18] allows the two-stage

butterfly switch unit to be operated by radix-2,-3,-4, -5,-8,-9, -12, -15, -16 and -25. This unit is built on a butterfly unit of the Radix-16 and is refashioned to fit the 2-, 3-, 4-, 5-, 8- and 16-point radics according to Spatial Design Exploration Section II. It has two PE-A units, a PE-B unit, two PE-C units and several switch networks. As seen in Fig. 3. The butterfly unit is supported by one radix-16, two radix-5/8 simultaneously, four radix-3/4 at once or eight radical-2 simultaneous operations. In Fig. 3, radix-2, — 4,-8 and -16 support the operation PE-A, one part A supports radix-5 DFT operations or two part A support operations for radix-3 DFT. The device may also be operated in one component A.

A PE-C unit supports two operations in Radic-4 radix-16 FFT, one part C in Radic-6 FFT or two part C in Radio-3 DFT operations in Radic-8 FFT operation. The PE-B unit covers all non-trivial multipliers of radix 3, -5, -8 and -16 as well as the add-ons for part B of the computing of radix-5. The Single Path Delay feedback (SDF, for its Spanish initials), reduces the number of multipliers, but complicates and makes memory user-friendly while MDC saves more area[5]. The multilinear delay commenter (MDC) utilizes memory and switch boxes to offer forward stream feedback channels. Multipath Delay Commenter and Memory Schedule are used to execute Furier transformation rapidly for the numerous inputs of the orthogonal frequency divisions of various lengths. The observation in the design list indicates that the memory-related feedback architecture is more effective than the delay commentator counterpart. We require a twelfth factor for calculating FFT, to allow us to generate numerous input signals and to that effect a huge ROM size with 20 factors has to be stored, raising expenses. This displays the FFT/IFFT processor that eliminates the twin factor of the ROM. For switching and adding operations, the complex multipliers are used, thus the CPU uses a two-input digital multiplier that does not have to stow a factor two, as with the ROM. The design is also a twelfth factor constant multiplier, which may be reconfigured and complex, rather than using ROM.

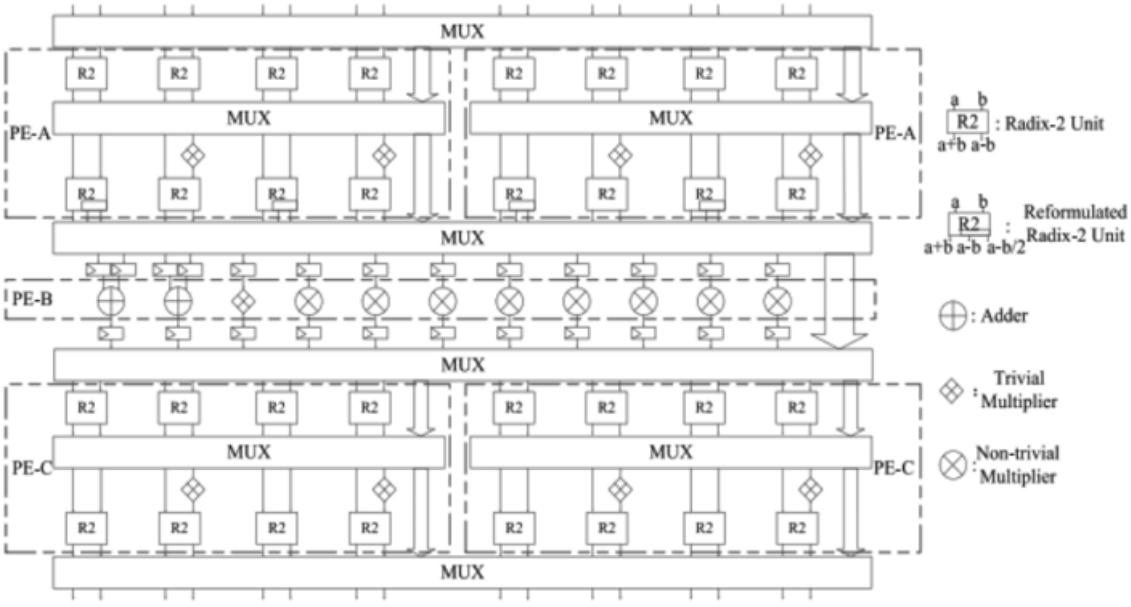

FIG. 3. BUTTER FLY UNIT IN PROCESSING ELEMENT.

RESULTS AND DISCUSSION

The RTL and RTL internal scheme, as shown in the images below, are displayed and the table columns 1 and 2 summarize numerous parameters.

RTL BLOCK DIAGRAM

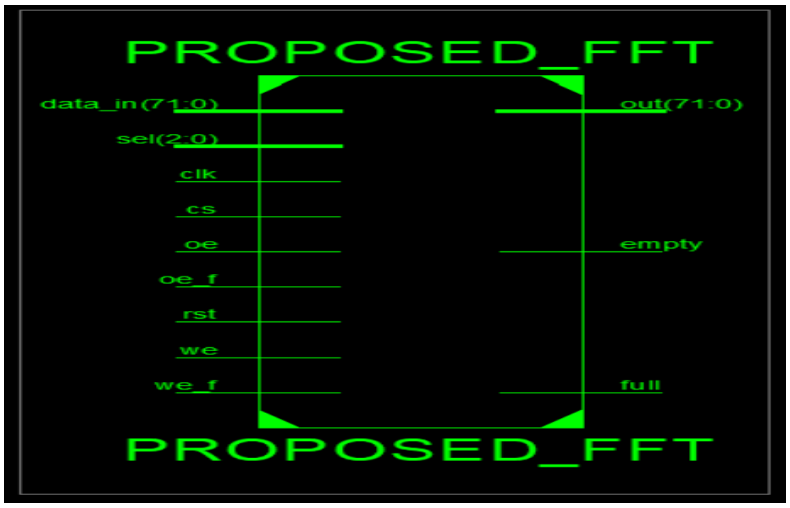

FIGURE 4: SCHEMATIC DIAGRAM OF PROPOSED FFT

INTERNAL BLOCK DIAGRAM

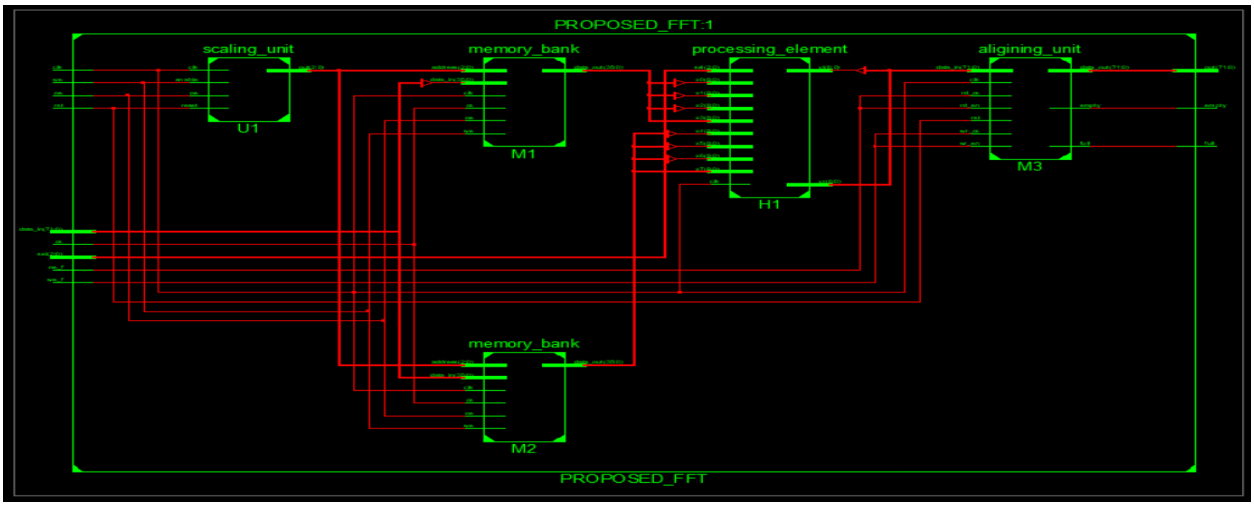

FIG 5: INTERNAL BLOCK DIAGRAM OF FFT SYSTEM

SIMULATION RESULTS

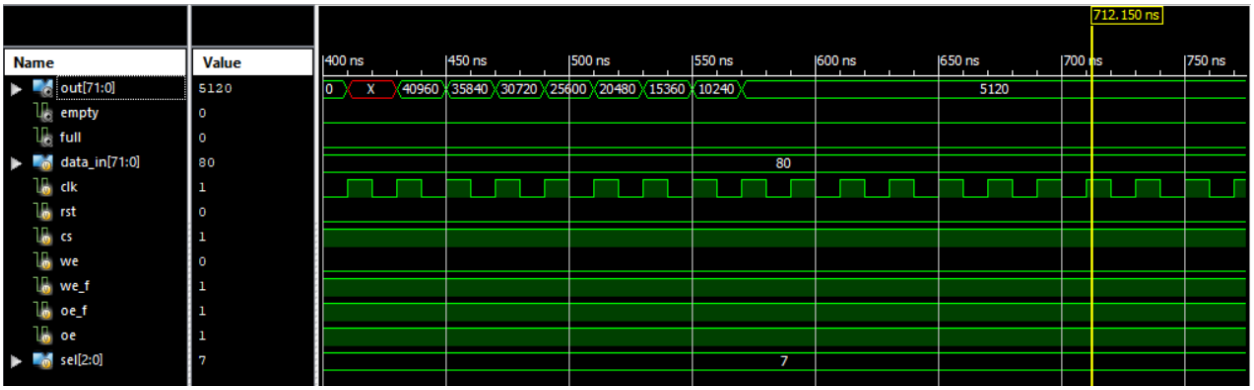

FIGURE 6: SIMULATION FOR PROPOSED FFT SYSTEM

COMPRESSION TABLE-1

Proposed method	Delay 5.674ns	Area 450 LUTS
Extension method	5.382ns	1,114 LUTS

CONCLUSION

In this article we have suggested an MDC MIMO FFT/IFFT processor based on radixr for processing parallel input streams of Ns, where r = Ns for attaining a use rate of 100%. The suggested method is appropriate for the processor of MIMO-OFDM basebands like WiMAX or LTE applications, with 2048, 512, 256 and 128 configurations of Ns = 4. We also suggested an effective schedule for memory to be used in full. It significantly reduces the chip size since an FFT/IFFT processor typically has a memory need above the chip area. The suggested design is based on an MDC architecture that is usually not favorite since the memory use rate and computer components like adders and multipliers are small. It is worth noting. The proposed memory scheduling, however, has proven to be an encode architecture suitable in MIMO-OFDM systems for FFT/IFFT processors because butterflies and multipliers are capable of achieving a usage rate of 100%, while maintaining in the design proposed the features of a simplicity of encoding control.

FUTURE SCOPE

We can implement this processing into data into mobile and another communication devices with low memory usages in communication systems and also used for security image transmission.

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