Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 7, July 2021: 10692 - 10696

Research Article

Low Complexity Ldpc Codec For 802.16e Standard

[1] Channaveeramma.E, [2]K.M.Palaniswamy

Abstract

The WiMAX is an IEEE 802.16e wireless communication standard used in wireless MAN's use LDPC codes as the error correcting codes. The throughput requirements of WiMAX standard is 75Mbps demanding high number of arithmetic operations and increased memory accesses per second. In this paper the dual diagonal structured LDPC encoder is used which reduces the encoding complexity. Horizontal TDMP Min-Sum algorithm is used for the decoding which halves the number of iterations and also leads to reduced memory footprint.

Keywords: LDPC, wireless MAN, TDMP, WiMAX.

1. Introduction

Low-density parity-check (LDPC) codes [1][2] have attracted much attention in the last decade due to their capacity-approaching error correcting performance. LDPC codes suffer from high encoding complexity. The complexity of directly encoding by using the generator matrix is quadratic in the block length of the LDPC code. The dual diagonal structure of LDPC codes reduces the encoding complexity[3] and hence adopted in wireless metropolitan area network (MAN) standard, WiMAX standard. The approach given in [4] can encode this class of codes in near-linear time, and the sequential method proposed in [5] can encode them in linear time. For dual-diagonal LDPC codes, another effective encoding approach [10][11] is based on arbitrary bit creation and correction. This method provides low encoding complexity while also reducing the number of cycles necessary to encode each code word.

To rectify the parity bits, the matrix structure is used in the encoding process. However, their method cannot be used to encode IEEE 802.11n or 802.16e LDPC codes directly. When adopting this approach, you'll need to change the matrix structure. According to their findings in [11,] this alteration degrades performance and increases error floors as compared to the original 802.11n dual-diagonal configuration. A generalized encoding scheme based on the technique of parity bit prediction and correction is proposed in this paper. The proposed scheme can be directly applied to encode IEEE 802.11n and 802.16e dual-diagonal LDPC codes without any changes in the matrix.

[1]Department of Electronics and Communication Engineering, Navodaya Institute of Technology, Raichur, Karnataka.
[2]Department of Electronics and Communication Engineering, Dr. T. Thimmaiah Institute of Technology, Ooragum, Kolar Gold Fields, Karnataka.
[1]Channaveeramma.e@navodaya.edu.in, [2] drpalaniswamy@drttit.edu.in

Layered scheduling, also known as Turbo Decoding Message-Passing (TDMP) techniques, allows for a two-fold increase in decoding convergence speed. [12] described a layered-based scheduling technique known as horizontal-layered scheduling. We concentrated on horizontal-layered scheduling, which is less difficult than vertical-layered scheduling [13].

The rest of the paper is arranged as follows. The section 2 consists of the methodology used, section 3 contains the results and discussion and finally conclusion and references in the sections 4 and 5.

2. Methodology

Proposed Encoding scheme:

Step_1._Set p0’ (i.e., b0, b1, …, bz-1) as any binary vector.

Step_2._Compute the vector $\lambda = H_s s$ by circularly shifting and accumulating the subblocks of s. (We denote $\lambda = [c_0\ c_1\ \ldots\ c_{m-1}]$ and $\lambda_i = [c_{iz}\ c_{iz}+1\ \ldots\ c_{(i+1)z-1}]$ for i = 0, 1, …, mb-1)

Step_3._[Forward Derivation] Compute p_1’, p_2’, … , p_x’.

Step_4._[Backward Derivation] Compute p_{mb-1}’, p_{mb-2}’ … , $p_{x+1'}$ and p_y.

Step_5._Compute p_0 by adding $p_{x'}$, and p_y.

Step_6._Compute the correction vector **f** by circularly shifting the sum of p_0 and p_0’ to the left by d positions.

Step_7._[Correction] If **f** is a nonzero vector, then compute $\mathbf{p_i}$ by adding $\mathbf{p_i}$**’** and f for i = 1 to mb-1. Otherwise, $\mathbf{p_i}$ is simply $\mathbf{p_i}$’.

In Step 1, p_0’ is set arbitrarily instead of being computed by the matrix operations. The following steps can directly proceed without waiting for the complicated computation of p_0. The parity subblocks p_1', p_2',..., $p_{mb-1'}$ can therefore be retrieved without knowing exactly what p_0 is in Steps 3 and 4. In Step 5 and Step 6, p0 and the correction vector f are calculated. The proposed encoding method has the advantage of low encoding delay because deriving the solutions of p_1, p_2, …, p_{mb-1} starts earlier without computing p_0 first. In addition, there is no dependence between Step 3 and Step 4, so forward and backward derivation can be executed simultaneously. Our technique minimizes the encoding time even more because the algorithm provided in [8] can only create these bits using forward substitution.

1/2, 2/3A, 2/3B, 3/4A, and 5/6 code rates are currently supported by the encoder. The 3/4B matrix's base matrix is not implemented since it is constructed differently from the others. All of the block sizes provided in the 802.16e standard are supported by the encoder. Algorithm 1 provides a formalization of the TDMP scheduling using the Min-Sum approximation. The two processing kernels of the flooding-based technique (one for CN processing and the other for VN processing) are combined in TDMP scheduling (kernel 2 in Algorithm 1). The kernel that results is known as CN centric. The overall computations required to evaluate a CN and the up-to-date of its linked VNs are executed concurrently during a kernel 2 loop. In terms of algorithmic efficiency, TDMP scheduling has several advantages over flooded scheduling [9].

Kernel 1: Initialization
for all $m \in C, n \in \Psi(m)$ **do**
  $L_{mn}^{(0)} = 0$
end for
$\triangleright$ *Process* $iter\_max$ *decoding iterations*
for all $t = 1 \rightarrow (iter\_max)$ **do**
  Kernel 2: For each check node in the code
  for all $m \in C$ **do**
    $\triangleright$ *Compute* L_{nm} *message*
    for all $n \in \Psi(m)$ **do**
      $L_{nm}^{(t)} = E_n - L_{mn}^{(t-1)}$
    end for
    $\triangleright$ *Compute* L_{mn} *message*
    for all $n \in \Psi(m)$ **do**
      $sign(L_{mn}^{t}) = \left[\prod_{(n' \in \Psi(m)/n)} sign(L_{n'm}^{(t)}) \right]$
      $|L_{mn}^{t}| = \left[\min_{(n' \in \Psi(m)/n)} |L_{n'm}^{(t)}| \right]$
    end for
    $\triangleright$ *Immediately update* E_n
    for all $n \in \Psi(m)$ **do**
      $E_n = L_{nm}^{t} + L_{mn}^{t}$
    end for
  end for
end for
Kernel 3: Hard decision
for all $n \in V$ **do**
  $\hat{c}_n = \begin{cases} 0 & \text{if } E_n \le 0 \\ 1 & \text{if } E_n > 0 \end{cases}$
end for

To begin, divide the number of decoding iterations required to obtain equivalent correction performance by two [11]. As a result, both the number of memory accesses and the complexity of the computation are divided by two. Second, the TDMP technique decreases the memory footprint by around 40% [11]. The L_{nm} messages are not saved in memory in the TDMP algorithm; instead, they are computed on the fly during the decoding process.

The Turbo-Decoding Message-Passing Algorithm is used by the decoder. The 1/2, 2/3A, 2/3B, 3/4A, 3/4B, and 5/6 code rates are currently supported by the decoder. All of the block sizes offered in the 802.16e standard are supported by the decoder.

3. Results and Discussion

The simulation results show the BER curve for LDPC codes with rate ½ and various N values of WiMax standard 802.16e. In fig.1, we observe that the bit error rate of $7.34\text{x}10^{-8}$ for N=576 and k=288. Fig.2 shows $5.67\text{x}10^{-8}$ for N=2304 and k=1152. Fig.3 shows $2.36\text{x}10^{-6}$ for N=2304 and k=1536 that is rate 2/3A. Fig.4 shows $2.36\text{x}10^{-6}$ for N=576 and k=480, rate 5/6 of the WiMax 802.16e standard. Fig.5 shows the WiMax LDPC code performance as compared with the Shannon bound and observed that the LDPC codes are the capacity approaching codes.

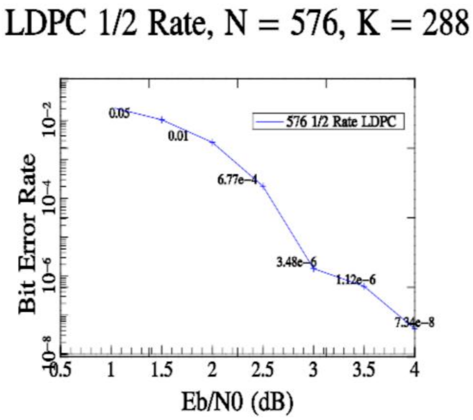

Figure1: BER curve for LDPC Rate ½. N=576, K=288.

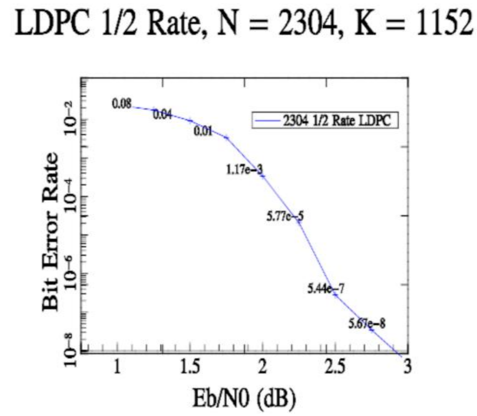

Figure 2: BER curve for LDPC Rate ½. N=2304, K=1152.

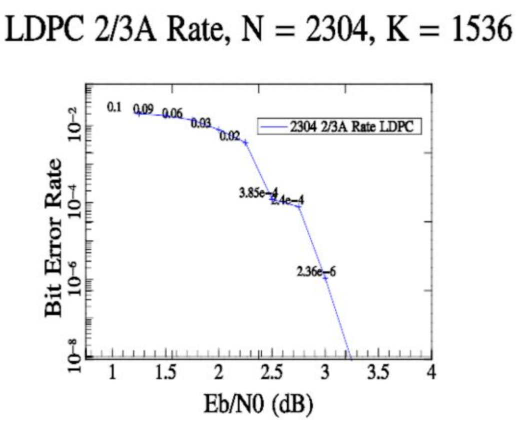

Figure 3: BER curve for LDPC Rate 2/3. N=2304, K=1536.

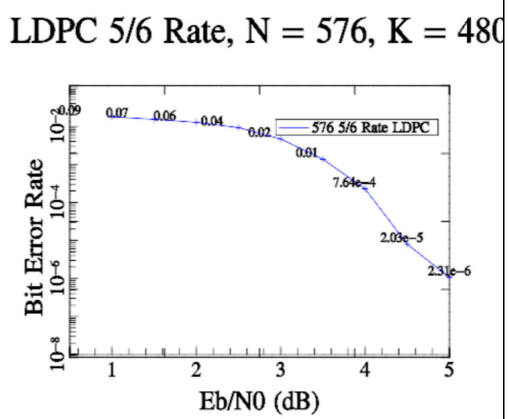

Figure 4: BER curve for LDPC Rate 5/6. N=576, K=288.

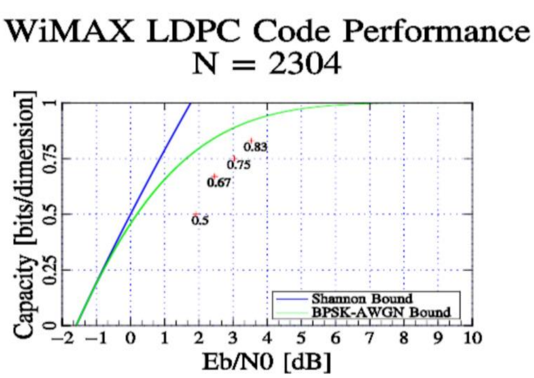

Figure.5 WiMax LDPC Code Performance for BPSK -AWGN, N=2304, rate ½.

4. Conclusion

In this paper the dual diagonal structured LDPC encoder is used which reduces the encoding complexity. Horizontal TDMP Min-Sum algorithm is used for the decoding which halves the number of iterations and also leads to reduced memory footprint.

5. References

5.1. Journal Article

1. R. G. Gallager, “Low density parity check codes,” IRE Trans. Inform. Theory, vol. IT-8, pp. 21–28, Jan. 1962.
2. D. J. C. MacKay and R. M. Neal, “Near Shannon limit performance of low density parity check codes,” Electron. Lett., vol. 32, p. 1645, 1996.
3. IEEE P802.11nTM/D2.00, “Draft STANDARD for information technology, telecommunications and information exchange between systems, local and metropolitan area networks, specific requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Enhancements for Higher Throughput,” IEEE 802.11 document, Feb. 2007.
4. T.J. Richardson and R.L. Urbanke, “Efficient encoding of low-density parity-check codes,” IEEE Trans. Inform. Theory, vol.47, no.2 pp. 638- 656, Feb. 2001.
5. Z. Cai, J. Hao, P.H. Tan, S. Sun, and P.S. Chin, “Efficient encoding of IEEE 802.11n LDPC codes,” Electronics Letters, vol. 42, no. 25, pp. 1471-1472, Dec. 2006.
6. F. Guilloud, E. Boutillon, J. Tousch, and J.-L. Danger, “Generic description and synthesis of LDPC decoders,” IEEE Transactions on Communications, vol. 55, no. 11, pp. 2084–2091, 2007.
7. G. Falcao, J. Andrade, V. Silva, and L. Sousa, “GPU-based DVB-S2 LDPC decoder with high throughput and fast error floor detection,” Electronics Letters, vol. 47, no. 9, pp. 542–543, 2011.
8. S. Kopparthi and D. M. Gruenbacher, “Implementation of a flexible encoder for structured low-density parity-check codes,” IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PacRim 2007), pp.438-441, Aug. 2007.
9. F. Guilloud, E. Boutillon, J. Tousch, and J.-L. Danger, “Generic description and synthesis of LDPC decoders,” IEEE Transactions on Communications, vol. 55, no. 11, pp. 2084–2091, 2007
10. Hongwei Song, Jingfeng Liu and B. V. K. V. Kumar, "Low complexity LDPC codes for partial response channels," Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE, 2002, pp. 1294-1299 vol.2, doi: 10.1109/GLOCOM.2002.1188406.

5.2. Conference Proceedings

1. C. Yoon, E. Choi, M. Cheong, and S.-K. Lee, “Arbitrary bit generation and correction technique for encoding QC-LDPC codes with dualdiagonal parity structure,” IEEE Wireless Communications and Networking Conference, (WCNC 2007), pp. 662-666, March 2007.
2. C. Yoon, J.-E. Oh, M. Cheong, and S.-K. Lee, “A hardware efficient LDPC encoding scheme for exploiting decoder structure and resources,” IEEE Vehicular Technology Conference (VTC2007-Spring), pp. 2445- 2449, April 2007.
3. D. E. Hocevar, “A reduced complexity decoder architecture via layered decoding of LDPC codes,” in Proc. of the SIPS Workshop, 2004, pp. 107–112.
4. M. Li, C. A. Nour, C. Jego, and C. Douillard, “Design and fpga prototyping of a bit-interleaved coded modulation receiver for the dvb-t2 standard,” in Proceedings of the SiPS conference, 2010.