

Design and Comparison of 16X16 Reversible VedicMultiplier using Different Adders

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Abstract

In this paper we have designed and analyzed 16-bit Vedic Multiplier using Ripple Carry Adder(RCA) , Carry Look- Ahead Adder(CLA) and Carry Select Adder(CSA). The design was simulated using Xilinx ISE design suite 14.7 and ModelSim 6.3g . The area and speed of the Reversible Vedic Multiplier using different Adders are compared. Carry Look Ahead Adder with a different architecture having less number of Reversible Logic Gates and garbage outputs are designed.

Index Terms

Reversible Logic Gate, Ripple Carry Adder, Carry Look Ahead Adder, Multiplier, Vedic Multiplier, Carry Select Adder.

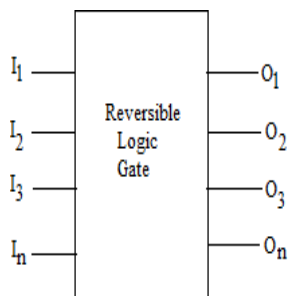


Fig. 1. Reversible Logic Gate

INTRODUCTION

The technology is advancing at a faster pace and due to miniaturization; area occupied by the chip and the speed of the circuit is the main concern. Multipliers are the main modules that decide the system over all propagation delay. Vedic multipliers are the fastest multipliers when compared to other multipliers. Urdva Triyagbhyam is the technique that is implemented in the Vedic multipliers. Since ideally there is zero power dissipation for reversible logic gates , in our design we are implementing Vedic multipliers in reversible logic.

I. REVERSIBLE LOGIC GATES

Reversible Logic Gates are the Basic Gates whose input vector is equal to output Vector. The input can be reproduced from the output and hence the name Reversible Logic Gates. Reversible Logic Gates have various applications in CMOS technology, and in different computing technologies like quantum, optical and DNA computing etc.,The only problem with the Reversible Logic Gate is the no of garbage outputs. The Reversible Logic Gates have power dissipation ideally of zero . The following are few basic Reversible Logic Gates which are used in our design.

HNG Gate

The 4*4 HNG Gate shown in the figure 2. The inputs are A,B,Cin,D and outputs are P,Q,R,S. In our design this gate is used in Ripple Carry Adders in place of full Adder. This is the main functionality of the HNG Gate. The Quantum cost is 6 for HNG gate .

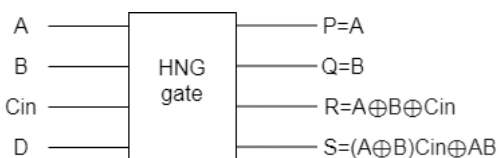


Fig. 2. HNG gate

A. PERES GATE

The figure 3 shows PERES gate . The inputs and outputs of the PERES gate is given as Input=(A,B,C) and output=(X,Y,Z) respectively.In our design the Peres gate is used in 2x2 Vedic multiplier and in CLA adder.The Quantum cost is 4 for Peres gate. Due to its low quantum cost is used in designing the half adder.

F. DPG GATE

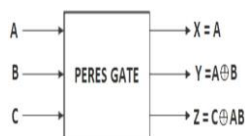


Fig. 3. Peres Gate

B. TOFFOLI GATE

The 4*4 DPG gate is shown in the figure 7. The DPG is known as Double Peres Gate. A,B,C,D are inputs and P,Q,R,S are outputs. Quantum cost of the DPG is 6.The DPG is used as the full adder and used in the Carry Select Adder in our design.

The figure 4 shows Toffoli gate. In our design the toffoli gate is used in CLA Adder. This gate has inputs A,B,C and outputs P,Q,R . Quantum cost is 5 for toffoli gate.

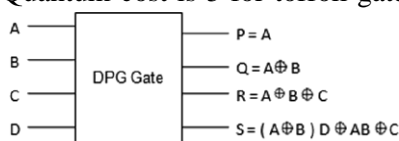


Fig. 4. Toffoli Gate

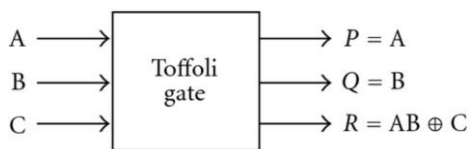


Fig. 7. DPG gate

II. RIPPLE CARRY ADDER

C. FEYNMAN GATE

Ripple carry adders are designed by cascading full adders. A n-bit adder will have n full adders. The carry-out of each full adder is the carry-in of the next adjacent full adder. Since the carry bits get rippled it is known as the Ripple carry adder.

The figure 5 shows Feynman Gate. This Feynman Gate is also called as CNOT Gate. The Feynman Gate has inputs A, B and outputs P, Q. Quantum Cost of the Feynman gate is 1. Feynman Gates are used in designing 2x2 Vedic Multiplier and Carry Look Ahead Adder.

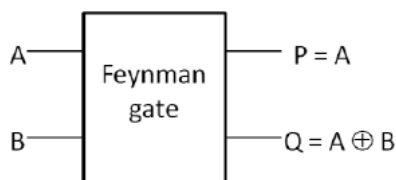


Fig. 5. Feynman gate

D. MFG GATE

MFG Gate is also called as Modified Fredkin Gate. The figure 6 shows the 3*3 MFG Gate. MFG Gate has inputs A, B, C and outputs P, Q, R. The Quantum Cost is 4 for MFG Gate. In our design MFG Gate is used as Multiplexer in Carry Select Adder.

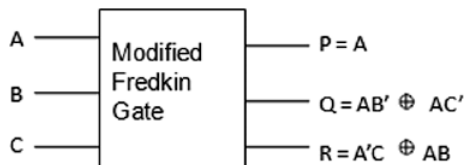


Fig. 6. MFG gate

Reversible Ripple carry adder is designed by using HNG gates which are cascaded to each other. The HNG gate acts as a full adder. The figure below shows Ripple carry adder of 4-bit by using Reversible logic.

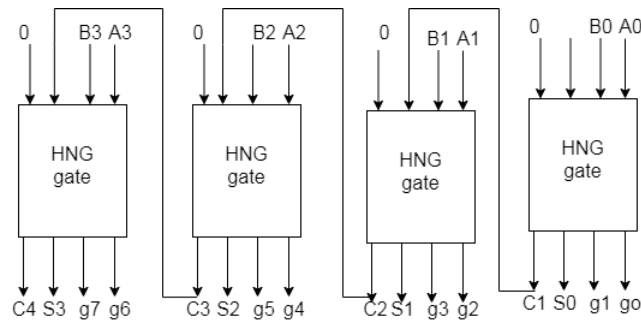


Fig. 8. 4 bit RCA.

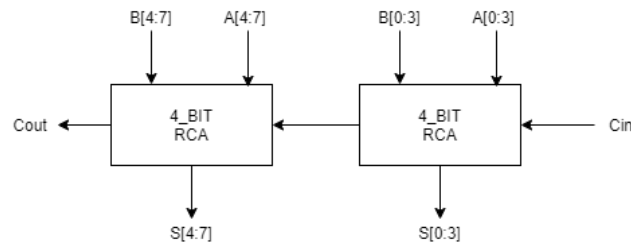


Fig. 9. 8bit RCA

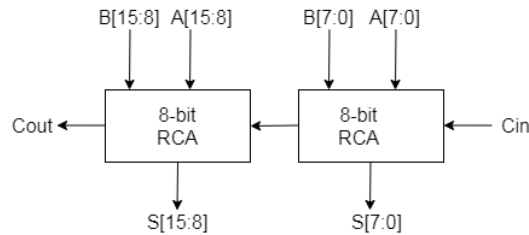


Fig. 10. 16bit RCA

III. CARRY SELECT ADDER

Carry select adder is most efficient adder than ripple carry adder. The delay of the carry select adder is lesser than ripple carry adder. It is simple but faster adder. The CSA generally consists of RCA and the multiplexer. In our design the DPG gates act as the full adders and the MFG gate acts as the multiplexer.

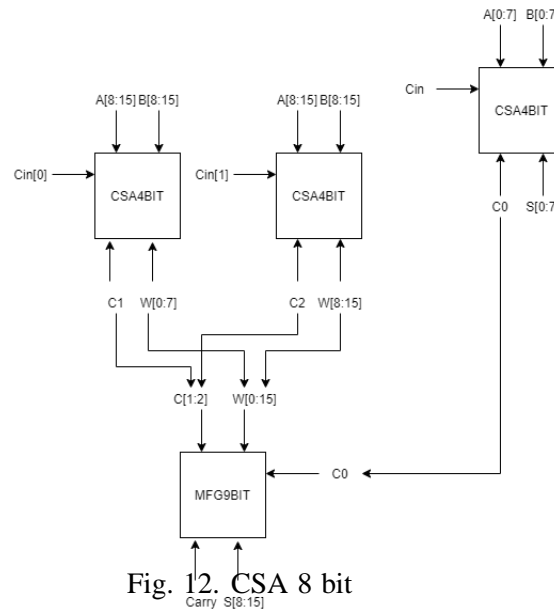


Fig. 12. CSA 8 bit

Based on selected line the respective input is selected. Since the MSB and LSB bits are computed individually the delay is comparatively reduced when compared with ripple carry adder. The 4 bit carry select adder is designed in reversible logic using (DPG) Double Peres Gate and (MFG) Modified Fredkin Gate . 4 bit carry select adder is as shown in the figure below. The below figures 12 shows carry select adder of 8 bit.

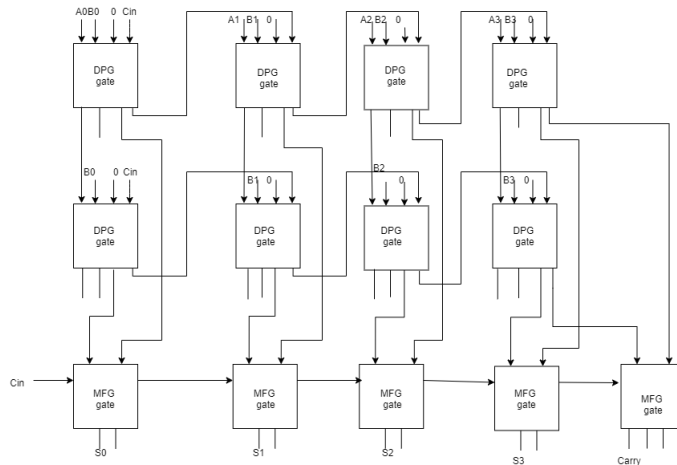


Fig. 11. CSA 4 bit

While adding the bits the LSB bits are given to the the adders which generate the carry out which is given as a selected line to the multiplexer.The MSB bits are added assuming one of the carry in as 1 and the other as 0. The sum and carry bits that or generated while adding the MSB bits is given to the the multiplexer as inputs.

CARRY LOOK AHEAD ADDER

This adder is also fast adder but the hardware is a bit more complex compared to the other two adders.The circuit becomes more complex when the bits are increasing. In the Carry look ahead adders sum is computed before carry is generated. This decreases the propagation delay of overall circuit which is the main advantage of this adder. Unlike in the ripple carry adder , the circuit of CLA doesn't have to wait for the carry to be propogated through all the stages. The carry input at any stage is independent of generated carry bits. So the carry bits can be generated at any time of the computation individually except for the intial stage carry bit. Carry propagation carry generation are resolved using the truth table. The Carry can be priory predicted and used for sum generation.The carry which is generated in the intial stage is used for the further carry generation.

Peres gates, feynman gates and toffoli gates are used in design of 4 bit reversible carry look ahead adder. The 4 bit carry look ahead adder using reversible logic gates is shown in figure below.The total number of the garbage outputs produced is 8 and the total number of gates used is 12, which is less compared to existing designs, and the total quantum cost of 4 bit CLA is 40. So the overall delay is reduced comapredto the existing design which uses peres and feynman gates.

In our design we have used three types of adders Peres gate ,Toffoli gate and Feynman gate four each. The figure belowrepresents the 4 bit CLA.

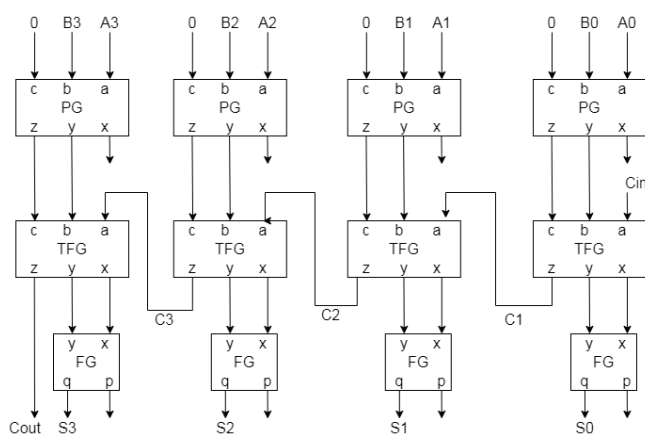


Fig. 13. CLA 4 bit

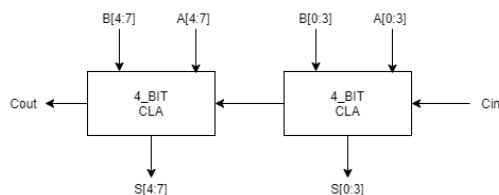


Fig. 14. CLA 8 bit

IV. MULTIPLIER

A combinational logic circuit which is used for the multiplication operation is called as the Multiplier. Multipliers play important role in (DSP) digital signal processing, FIR filtering, Image processing, Speech and Audio Processing etc., As the no of bits increases the computational circuit also increases. The multiplier architecture requires adders for the Multiplication operation.

V. VEDIC MULTIPLIER

Vedic multipliers the fastest multipliers when compared to array and booth multipliers. The multipliers of the main models which decide the delay of the system. So the Vedic multipliers every great advantage in reducing the overall propagation delay of the system. In our design 8x8 and 16x16 reversible Vedic multipliers using different types of adders like RCA, CLA and CSA are compared. The algorithm used in designing the vedic multiplier is Urdhva Triyagbhyam. There are around 16 types of there are algorithms in designing a Vedic multiplier but the above said technique is used for all kinds of multiplication purposes. The figures 18 and 19 represent the 8x8 and 16x16 vedic multiplier architecture. The adders used in the multiplier architecture can be replaced by any one of the three adders. The reversible 2x2 vedic multiplier is implemented by using peres gates and (CNOT gates)

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feynman gates. The below figure represents the reversible 2x2 vedic multiplier. The 8 x 8 vedic multiplier and 16x16 vedic multiplier design is shown in the fig 18 and 19 respectively.

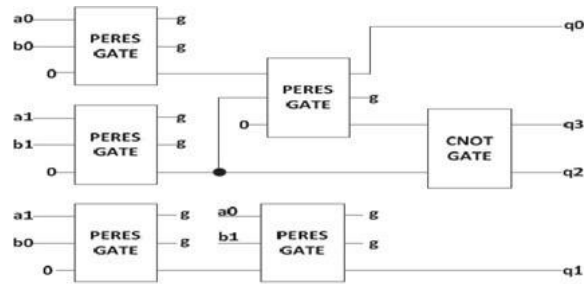


Fig. 15. 2x2 Vedic Multiplier

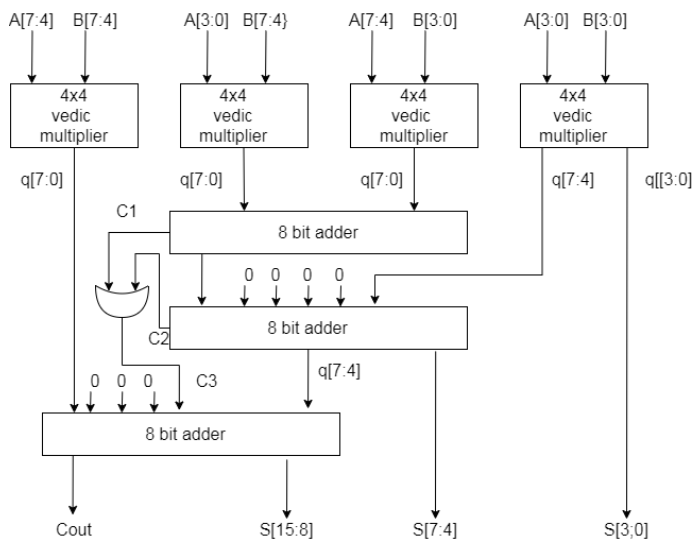


Fig. 16. 8x8 Vedic Multiplier

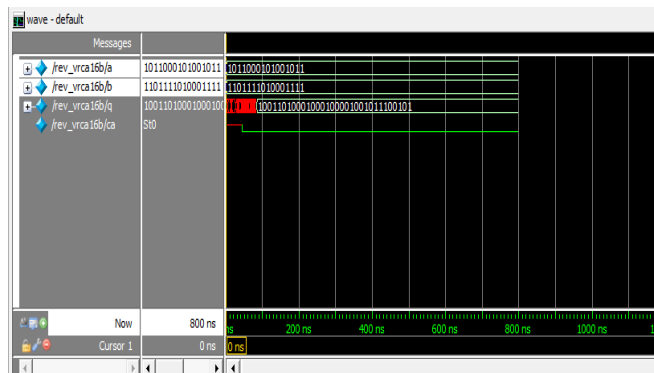


Fig. 19. 16x16 Vedic Multiplier using RCA

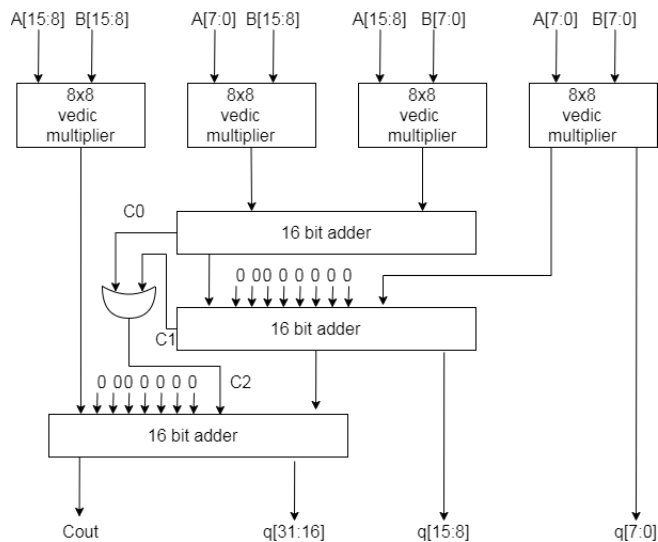


Fig. 17. 16x16 Vedic Multiplier

VI. METHODOLOGY

16x16 Reversible Vedic Multiplier is designed using different types of adders like Carry select adder, Ripple carry adder and Carry look ahead adder. The new architecture for the Carry look ahead adder is implemented. Comparison of reversible carry look ahead with the existing adder is given. The area and speed of 16-bit vedic multiplier is compared for the three different kinds of adders. The 16-bit vedic multiplier was modified in each architecture and then synthesized for results.

VII. SIMULATION RESULTS AND DISCUSSIONS

The following figures represent the simulation results of the 8x8 and 16x16 vedic multiplier using RCA, CSA and CLA.

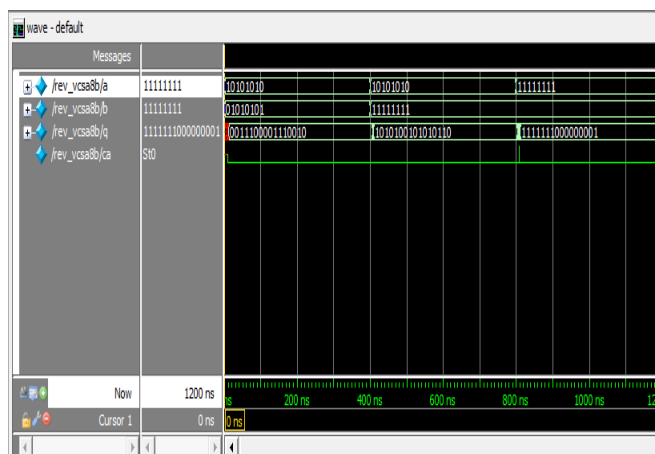


Fig. 20. 8x8 Vedic Multiplier using CSA

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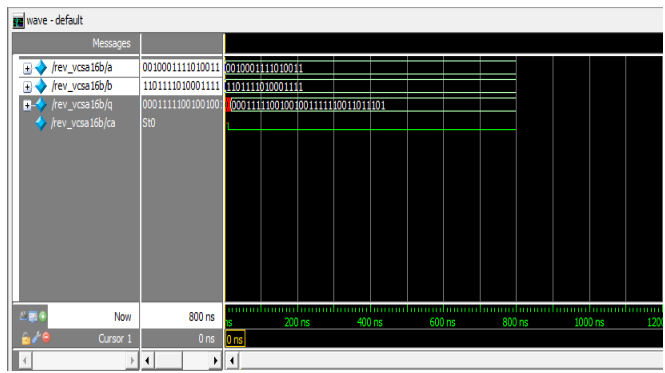


Fig. 21. 16x16 Vedic Multiplier using CSA

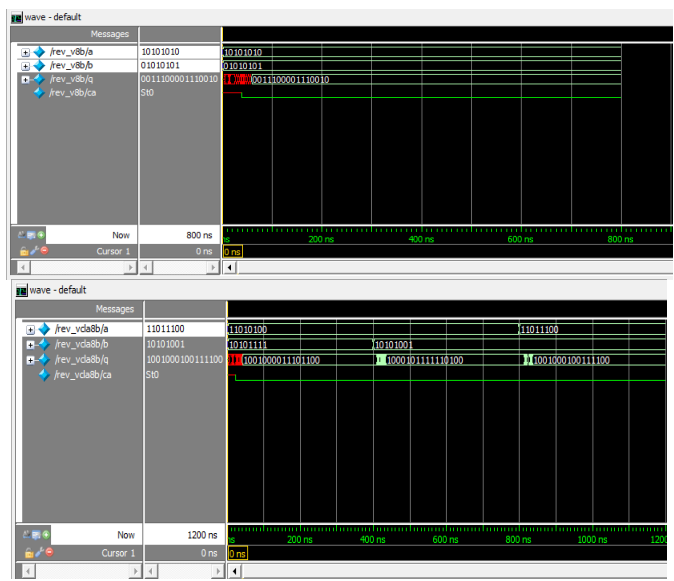


Fig. 22. 8x8 Vedic Multiplier using CLA

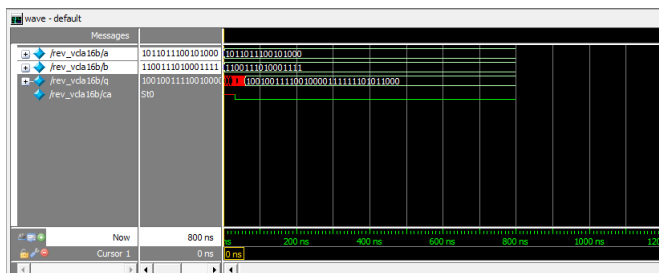


Fig. 19. 16x16 Vedic Multiplier using RCA

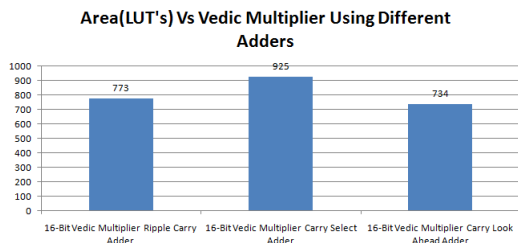


Fig. 23. 16x16 Vedic Multiplier using CLA

The below graphs represent the Comparative Analysis of Area and Delay for the 8x8 and 16x16 Reversible Vedic Multipliers using RCA, CSA and CLA.

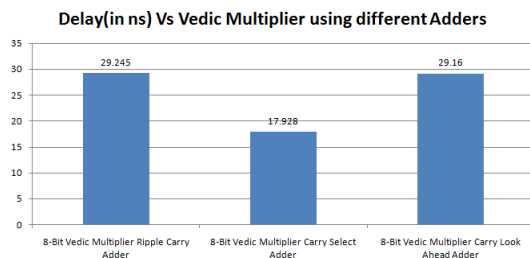


Fig. 24. Comparison of Delay for the implemented 8-bit Vedic Multiplier designs.

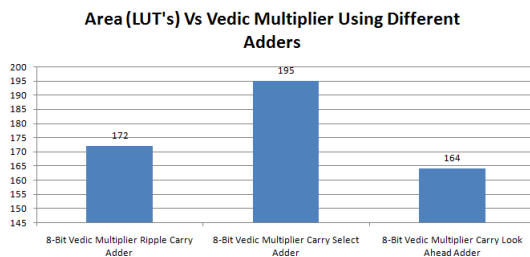


Fig. 25. Comparison of Area for the implemented 8-bit Vedic Multiplier designs.

Fig. 27. Comparison of Area for the implemented 16-bit Vedic Multiplier designs.

TABLE I
COMPARISON OF 4-BIT CARRY LOOK AHEAD ADDER

S.NO	WORK	NO OF GATES	QUANTUM COST	NO OF GARBAGE OUTPUTS
1	EXISTING	16	40	10
2	PROPOSED	12	40	8

TABLE II
AREA AND DELAY COMPARISON OF VEDIC MULTIPLIERS

S.NO	MULTIPLIER	LUT'S	DELAY(in nS)
1	8-Bit Vedic Multiplier using RCA	172	29.245
2	8-Bit Vedic Multiplier using CSA	195	17.928
3	8-Bit Vedic Multiplier using CLA	164	29.16
4	16-Bit Vedic Multiplier using RCA	773	50.811
5	16-Bit Vedic Multiplier using CSA	925	43.624
6	16-Bit Vedic Multiplier using CLA	734	51.271

	Multiplier using CLA		
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VIII. CONCLUSION

In our design Vedic multiplier of 16x16 using different adders like Carry Select Adder, Ripple Carry Adder and Carry Look-Ahead Adder(with new architecture) for reversible logic is proposed and analysed . The total no of garbage outputs and total no of gates required for (CLA) carry look ahead adder is low when compared with the existing work. It is observed that the delay is reduced 38.69% for 8x8 vedic multiplier and 14.14% for 16x16 Vedic multiplier using CSA as compared to RCA.

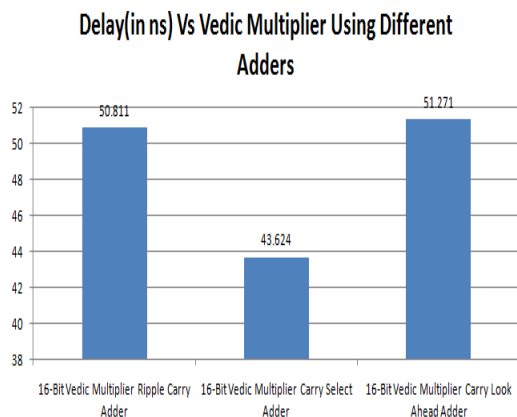


Fig. 26. Comparison of Delay for the implemented 16-bit Vedic Multiplier designs.

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