Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 9, August 2021: 1935 – 1947

Implementation of Modular Multilevel Converter and Cascaded H-Bridge using SPWM

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Abstract:

The large inverters are satisfied the expanding demand of medium and high power industrial applications, present which are reach out to hundreds of megawatt power. Connect solitary one power semiconductor switch openly to the grid owing to the high voltage variety, currently it is very challenging. Multilevel Inverters (MLI) are use elevated speed switching components, so they are avoiding that complication of connecting them straight to the network by hooking solitary devices among manifold DC stages. This paper deals with comparative analysis and design of the Cascaded-H-Bridge (CHB) Multilevel Inverter and Modular Multilevel Converter (MMC).The main objective of this paper is to analyze the performance of Cascaded-H-Bridge MLI and Modular Multilevel Converter for different levels of voltage by using sinusoidal pulse with modulation**(**SPWM**)** techniques like in phase disposition (IPD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD)and to find out which Modulation technique will give better THD and improve efficiency of converterby using MATLAB/SIMULINKsimulations.

Keywords: *MMC Cascaded H Bridge Inverter, THD and MATLAB/Simulink.*

I. INTRODUCTION

Multilevel inverters are gaining importance in power industry for medium and high power applications. Multilevel inverter (MLI) converts DC power to AC power with desired levels. MLI has more advantages over the conventional inverters such as high efficiency, low switching losses and low harmonic distortion. MLI are used in numerous implementations; such as traction drives systems and high voltage direct current transmission (HVDC) [6] [8], flexible AC transmission systems (FACTS) [9], effectiveness interfaces for RES (fuel cells, photovoltaic and wind energy) and industrial motor drives [4]. Different types of MLI are diode clamped, flying capacitor and cascaded h-bridge.

Cascaded H-Bridge Inverter produce n level output voltages, it is using n-1/2 H-bridges. They are considered as medium voltage but high-power inverters [5]. The H-bridges are attached in a cascaded manner in order to get medium voltage output. Separate isolated DC supplies are needed to power the H-bridge network. The CHB Multilevel Inverter is very easy to compare with any other type of MLI because it need not require any clamping diodes and capacitors [2]. CHB is easy to install and to develop higher voltage levels but it needs many more switches and DC isolated sources

so overall there will be lesser switching losses and the filter used will be cheaper and smaller. So the system cost will be minimized.

MMC is one of the MLI topologies and it is suitable for HVDC and high power applications. MMC has many features than conventional MLI such as modularity, scalability, low power losses and low harmonic distortion.MMC has easy assembling and flexible converter model and it can provide for the two way flow of power[10]. MMC can get more number of output levels with lesser harmonic content and greater efficiency by Providing lower common-mode voltages and quality of power [3]. Its operation is transformer less as it provides high modularity and these results in lesser switching losses and elimination of the need of filtering.

II.CASCADED H-BRIDGEMULTILEVEL INVERTER

CHB MLI is another choice of the multilevel topologies. It is also denoted as series H-bridge converter. This MLI was utilized within a large range of demands. By means of it has flexibility as well as modularity, in high-power applications the CHB appears very dominance, particularly move and sequence associated flexible alternate current transmission systems monitor.CHB amalgamate owned product virtually stepped wave shapes by merging a lot of secluded voltage levels. As a result of adding up additional full bridge inverters, entirety of Van can be able to easily improved lacking decorate level of the voltage, as well as construct idleness beside each bridge of the converter breakdown could be noticed. ThischaracteristicisunfeasiblewithinsupplementaryVSCstructures utilize a frequent DC-link. From the time when this configuration contains the sequence of power exchange cells, the powerandvoltageintensitycouldbe simplyscaled.CHB MLI topology is formed on top of the series association of inverters through split DC sources. The voltages generated through the different modules with the consequential phase voltage are synthesized. The number of voltage level is based on the number of modules are used. The number of modules is equals to the number of dc sources, it is depends on the no of voltage levels.

$$M=N-1/2$$

Where
N =Number of output voltage levels
M = Number of modules

7-stage CHB inverter has three modules, each module generates the +Vdc, 0 and –Vdc the sum of the output voltage from each module different switching states are possible to generates +3Vdc, 0 and –3Vdc. The set of steps wave shape is almost AC, yet exclusive filtrate.Fig.1 shows the circuit model of N- level CHB multilevel.

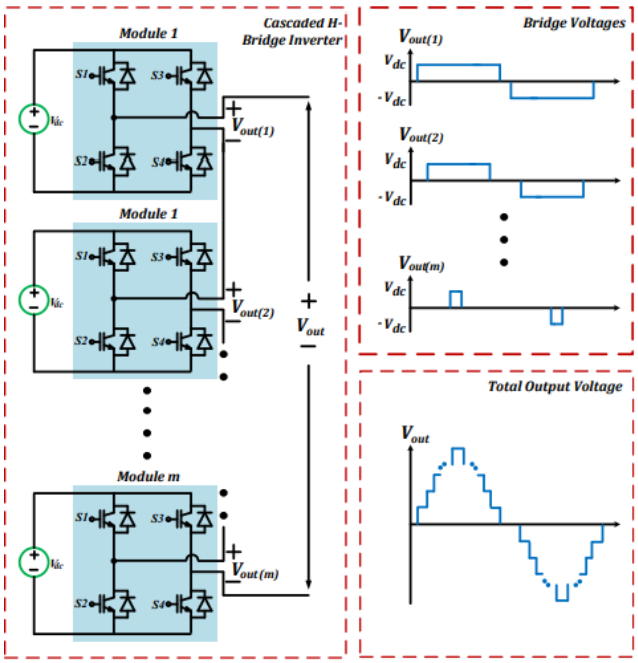


Fig1: Circuit diagrams of n-level CHB

In this MLI, the utilization of three separate H-bridge modules generates seven voltage levels at the load-side. For higher values, the load voltage is the aggregation of each module and it is expressed below

$$V_{out} = V_{01}+V_{02}+V_{03}\ldots\ldots\ldots\ldots V_{on}$$

The Fourier series of the output voltage for n-level has of only odd-order harmonics and it is defined as

$$V_o(t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,7\ldots}^{\infty} [\cos(n\alpha_1)+\cos(n\alpha_1)+\ldots+\cos(n\alpha_k)]\frac{\sin(n\omega_o t)}{n}$$

The coefficients are

$$V_n = \frac{4V_{dc}}{n\pi}[\cos(n\alpha_1)+\cos(n\alpha_2)+\ldots+\cos(n\alpha_k)]$$

The modulation index of the n-level CHB is

$$m = \frac{V_1}{S\left(4\times\frac{V_{dc}}{\pi}\right)} = \frac{\cos\alpha 1+\cos\alpha 2\ldots..cos\alpha s}{S}$$

The total harmonic distortion is

$$THD = \frac{\sqrt{V_{rms}{}^2-\left(\frac{AV_{dc}}{\sqrt{2}}\right)^2}}{\frac{AV_{dc}}{\sqrt{2}}}$$

III. MMC-MODULAR MULTILEVELCONVERTER

MMC is depending on the equal sub modules are connected in series. Every sub module has a distinguished HB (half-bridge) or full bridge configuration, half bridge contains two power semiconductors, IGBT and one sub module capacitor, full bridge consists of four IGBTs and one sub module capacitor. The output levels of the MMC is depend on the SM in the arm, n=2[N-1] where 'n' is number of SM in the MMC is depending on the equal sub modules are connected in series. Arm and N is no of resultant voltage stages.

These sub modules are consisted of half bridges and a diode in parallel in order to control the current flow. Each leg in one phase of the MMC has lower &upper arms. The arm voltage has controllable voltage source and then it produce the controllable voltage. Now the arm replaced by the controllable voltage sources. These sources are completely independent each other, this is the unique feature of the converter. Each leg in one phase of the MMC has lower &upper arms. It can be able to deduce that discharging and charging of SM capacitor happen as switch T1 is switched on. The capacitor is charging when the arm current is positive. Two transistors are off-state can characterize early demand of sub module capacitor during creation. The MMC has three operating states are blocking state, cut-in state and cut off state.

The sub module has two IGBTs T1 and T2 are work in a contradictory way. Avoid shoot-through the T1 is turned on, and must be turned off of the T2. The capacitor voltage (VC) appears at the SM terminals when T1 is switched on. During this situation, the SM is supposed in the direction ofsurvive"inserted" or "bypassed". The summarized operation of sub modules is mentioned in the table below:

Table 1: Summary of the operation of Sub modules

States	SM1	SM2	D1	D2	Capacitor
Blocking State	OFF	OFF	ON OFF	OFF ON	Inserted Not Inserted
Cut-in State	ON	OFF	-	-	Inserted

Here $V_o$is the resultantvoltage;V_{dc} is the applied DC voltage. Fig 2 shows the single leg of the MMC.

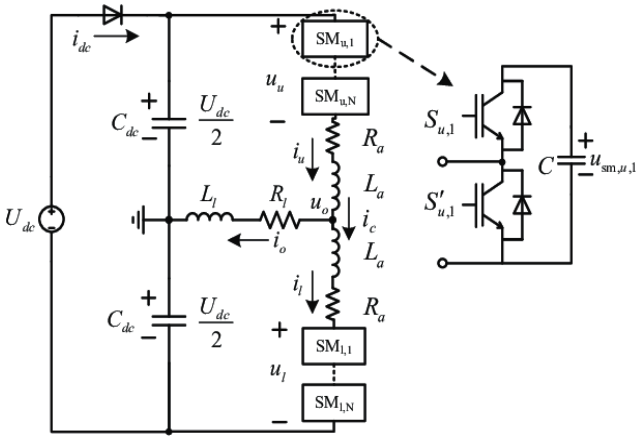


Fig2: Single legof MMC

Each leg in one phase of the MMC has lower &upper arms. Now the arm replaced by the controllable voltage sources.

$$V^*_{u(t)} = V_{dc}/2 \ [1 - mV_m \sin \omega t] \qquad \text{where } 0 \le m \le 1$$

$$V^*_{l(t)} = V_{dc}/2 \ [1 + mV_m \sin \omega t)]$$

Where m= modulation index is

$$\mathbf{m = 2V_m/V_{dc}}$$

The voltage rating of upper arm and lower arm is the total DC link voltage.

IV.PULSE WIDTH MODULATION TECHNIQUES

In this paper, the modulation technique used to power this inverter is Carrier deposition SPWM.Multi Carrier based modulation strategies are very compact and simpler, the most distinguished sinusoidal PWM strategies are In Phase Disposition -IPD,AlternativePhaseOpposition Disposition -APOD and Phase Opposition Disposition -POD.

In-phase deposition IPD

In this PWM all the carriers have identical phase disposition. In this strategy, a number of carriers are working within the solitary reference signal. The information of carrier waveforms is identical and the carriers are pre-arranged thus generating synchronized voltage levels. It is noticeable that the modulation index (MI) is equivalent to one (1) and the carrier frequency is 1000Hz in appearance form.

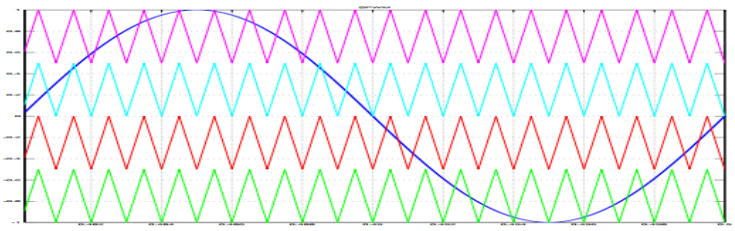


Fig 3: IPD Scheme

POD-Phase opposite deposition

In this PWM technique uses carriers in the negative (-) ve range of modulating signal those is 180◦ shifted as of the carriers within positive (+) ve range of the indication. In this carriers in above x-axis are within phase and those are π degrees out of phase below the x-axis. Fig 4 manifests the POD-SPWM scheme.

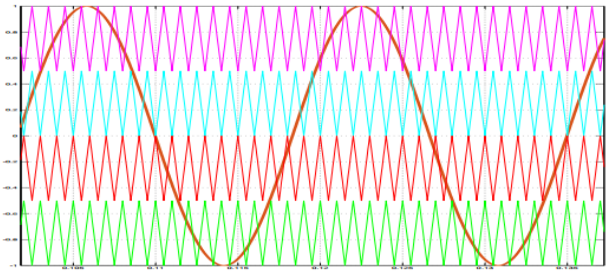


Fig 4:POD Scheme

Alternate Phase opposite deposition (APOD)

This technique, readily available isπ phase difference between the neighboring carrier signals. Fig5 shows APOD scheme.

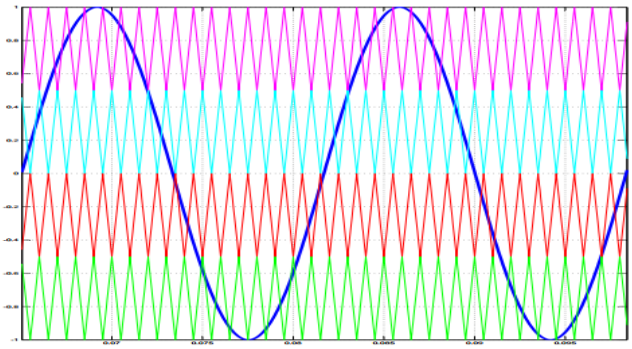


Figure 5: APOD scheme

V. THD ANALYSES OFMMC ANDCHB

The harmonic analysis of MMC and CHB are done by usingMATLAB/Simulink 2014a. These are compared in terms of total harmonic distortion for 3, 5, 7 and 9 levels.

Table 2 Design Parameters for CHB and MMC

S NO	Parameters	CHB	MMC
1	Input voltage	100	100
2	Load	100Ω	100Ω
3	Switching Frequency	1000kHz	1000khz
4	Arm inductor		0.01mH
5	Capacitor	2200µF	2200µF

For 3 stages

- The output voltage and THD for IPD, POD, and APOD strategies of three stages CHB are shown in fig 6, 7, 8, 9 respectively.

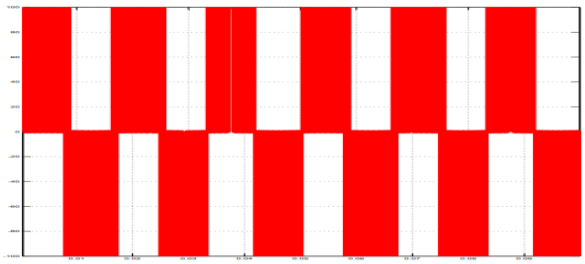


Fig 6:output voltage of the 3-stage CHB

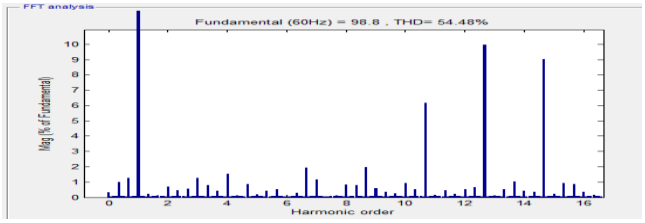


Fig 7:THD for 3-stage of CHB with IPD

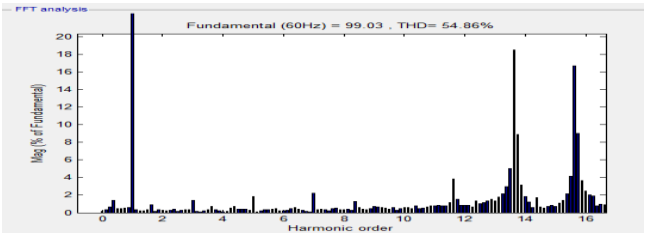


Fig 8:THD for 3-stage of CHB with POD

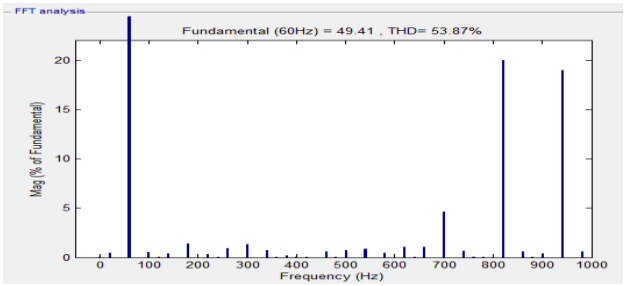


Fig 9:THD for 3-stage of CHB with APOD

Table 3 THD for the 3-level CHB

S NO	SPWM Schems	THD(%)
1	IPD	54.48
2	POD	54.86
3	APOD	53.87

- The output voltage and THD for IPD, POD, and APOD strategies of the three stages MMC are shown in fig10, 11.

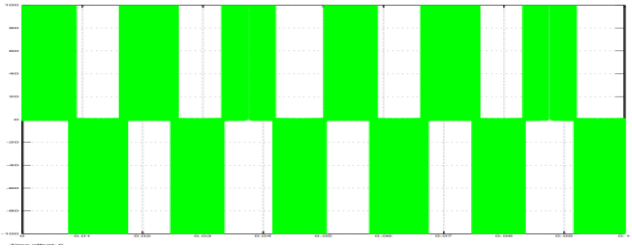
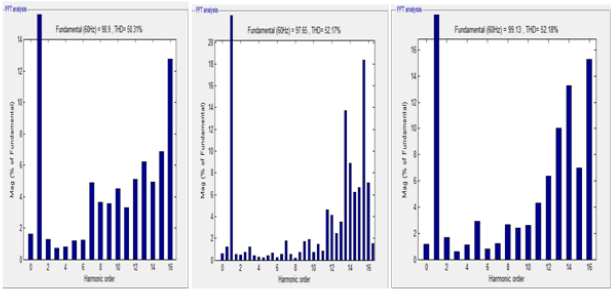


Fig 10:output voltage of the 3-stage MMC



IPD POD APOD

Fig 11:THD for the 3-level MMC of IPD, POD and APOD

Table 4 THD for the 3-level MMC

S NO	SPWM Schems	THD(%)
1	IPD	50.31
2	POD	52.15
3	APOD	52.18

For 5 Stages

- The output voltage and THD for IPD, POD, and APOD strategies of five stages CHB are viewed in fig12, 13 respectively.

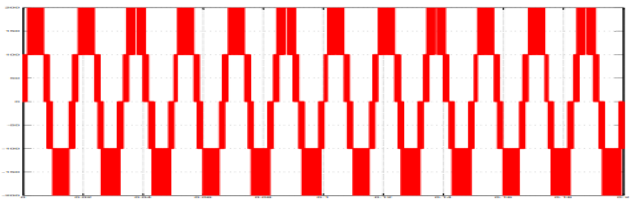
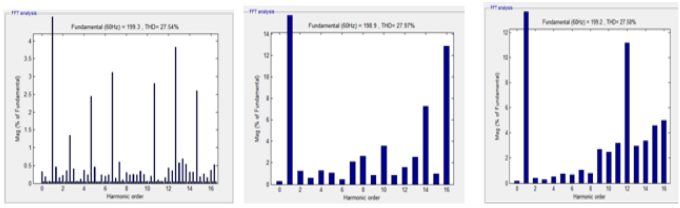


Fig12:output voltage of the 5-stage CHB



APOD POD IPD

Fig 13:THD for the 5-level CHB of IPD, POD and APOD

Table 5 THD for the 5-level CHB.

S NO	SPWM Schems	THD(%)
1	IPD	27.58
2	POD	27.97
3	APOD	27.54

- The output voltage and THD for IPD, POD, and APOD strategies of the five stages MMC are displayed in fig 14 and fig 15.

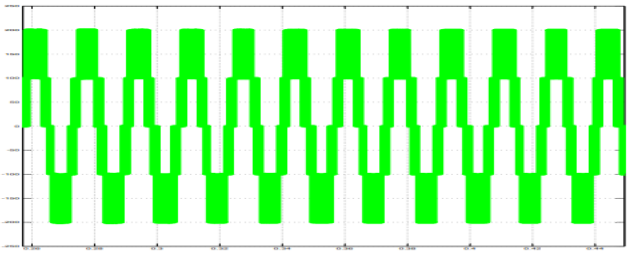
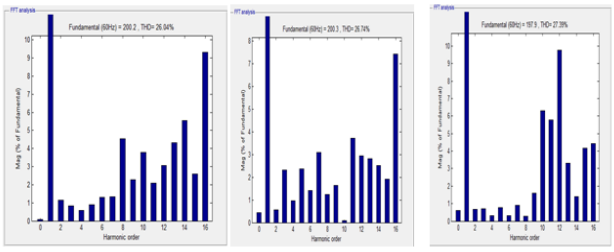


Fig 14: Output voltage of the 5-stage MMC



IPD POD APOD

Fig 15:THD of 5-stage MMC IPD, POD and APOD

Table 6 THD for the 5-level MMC.

S NO	SPWM Schems	THD(%)
1	IPD	26.04
2	POD	26.74
3	APOD	26.69

For 7 stages

- The output voltage and THD for IPD, POD, and APOD strategies of seven stages CHB are shown in

fig 16, 17 respectively.

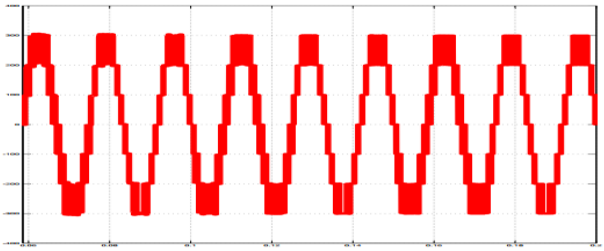
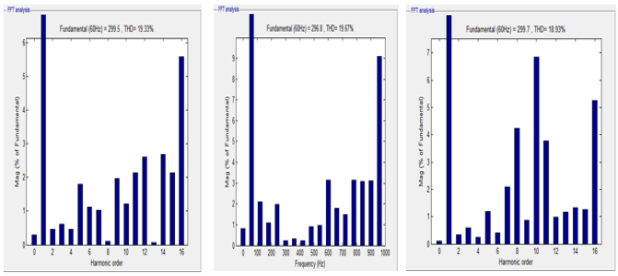


Fig 16:output voltage of the 7-stage



IPD POD APOD

Fig 17:THD for the 5-level CHB of IPD, POD and APOD

Table 7 THD for the 7-level CHB

S NO	SPWM Schems	THD(%)
1	IPD	19.33
2	POD	19.67
3	APOD	18.93

- The output voltage and THD for IPD, POD, and APOD strategies of the seven stages MMC are manifests in fig 18 and fig 19.

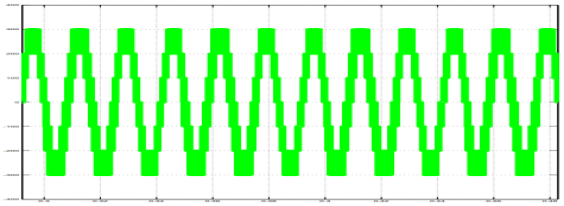


Fig 18:output voltage of the 7-stage MMC

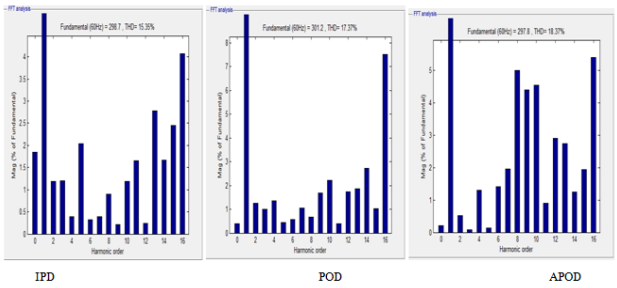


Fig 19:THD for the 7-stage MMC of IPD, POD and APOD

Table 8 THD for the 7-level MMC

S NO	SPWM Schems	THD(%)
1	IPD	15.33
2	POD	17.37
3	APOD	18.31

For 9 stages

- The output voltage and THD for IPD, POD, and APOD strategies of the nine stages CHB are viewed in fig20 and fig 21.

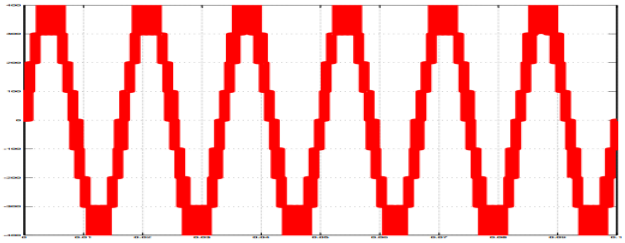


Fig 20:output voltage of the 9-stage CHB

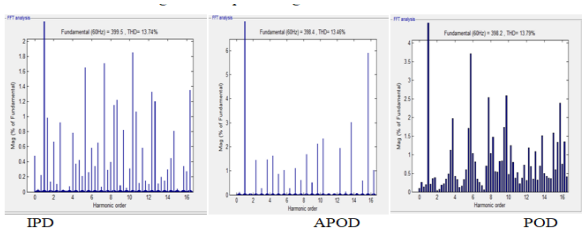


Fig 21:THD for the 7-stage CHB of IPD, POD and APOD

Table 9 THD for the 9-level CHB.

S NO	SPWM Schems	THD(%)
1	IPD	13.74
2	POD	13.79
3	APOD	13.46

The output voltage and THD for IPD, POD, and APOD strategies of the nine stages MMC are displayed in fig 22 and fig 23.

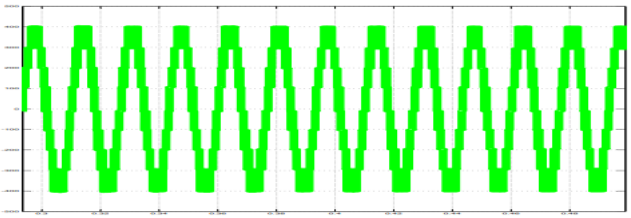


Fig 22:Resultant voltage of 9-stage MMC

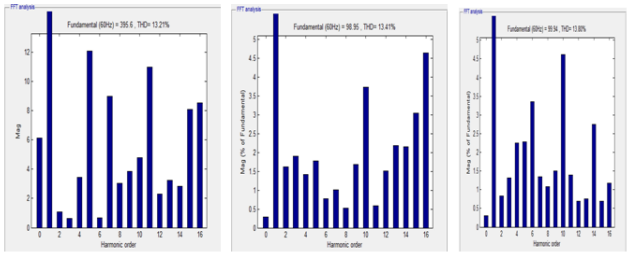


Fig 23: THD for the 9-stage CHB of IPD, POD and APOD

Table 10 THD for the 9-level MMC.

S NO	SPWM Schems	THD(%)
1	IPD	12.38
2	POD	13.03
3	APOD	13.80

VI. RESULTS

The results of comparative analysis, it is exposed that the APOD scheme used in Cascaded H-bridge having lesser THD in the output than IPD and POD schemes. While MMC is having THD as more effective compared with Cascaded H-bridge inverter implemented by using APOD scheme. The summarized results of the comparative analysis are given below in table 11 it is shown that IPD – PWM scheme used in MMC is having lower THD in the output than the APOD and POD Schemes. In every level MMC gives the better performance than the cascaded MLI. In every stage the magnitude of the harmonics are reduced for increasing the output voltage level.

Table 11Outline results of THD

Levels	CHB (APOD)	MMC (IPD)
3	53.87%	50.31%
5	27.54%	26.04%
7	18.93%	15.33%
9	13.46%	12.48%

VII. CONCLUSION

In this paper the operations of the MMC and CHB MLI by using SPWM approach with different voltage levels are studied. All circuit models of CHB &modular multilevel converter are simulated in MATLAB/SIMULINK. From the simulated results it is concluded that 9-level, 7-level, 5-level and 3-stage CHB Inverters produce lesser THD when it is used with APOD modulation scheme. The MMC gives the very good THD with compared to the H- Bridge MLI using the same modulation strategies. The operation of the MMC is better than the cascaded H-bridge MLI because it has excellent features like Redundancy and reliability, Modularity and scalability to different power and voltage stages, Compatibility with commercial semiconductors, High efficiency and High capacity of the resultant voltages. From the results the harmonics were considerably low in 9-level of MMC&CHB when compared with other designed levels and it is reduced at the output voltage to increasing the number of levels and preferred alternating voltage level is obtained.

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