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Implementation of bm3d mri denoising equipped with noise invalidation technique using fpga.

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Abstract— Magnetic Resonance Images (MRI) widely used for diagnosis and the treatment of brain tumours. It is the most powerful imaging technique developed to study the structural features of the internal body parts. MR images are affected by artefacts and noise that is adequately modelled as Rician noise. Image denoising plays an important role in MRI. In this paper BM3D algorithm is implemented with Noise Invalidation Denoising (NIDe) technique on FPGA. Noise Invalidation Denoising (NIDe) technique gives the optimum threshold value automatically based on the data and noise characteristics over hard thresholding. Variance Stabilization Transform (VST) applied before denoising which removes the dependency of the noise variance on the MRI image intensities. Experiments perform on metrics such as peak signal to noise ratio (PSNR) and structural similarity index (SSIM). FPGA implementation clearly shows the advantages over its Matlab implementation. This algorithm is coded in VHDL and can be simulated using ModelSim.

Keywords: Block-matching and 3D filtering, Magnetic resonance imaging, Denoising, Noise invalidation denoising, Variance stabilization transform, FPGA

I. INTRODUCTION

Medical field uses MRI images for capturing images of different body parts. These images provide more granular details about human body parts, which help medical professionals in accurate diagnosis and treatment. Different medical imaging modalities used in modern medicine are X-rays, Computed Tomography, Nuclear imaging, Magnetic Resonance Imaging and Ultrasound developed for number of applications. These captured images generally had to deal with unwanted additional noise. Noise is the unwanted signal that interferes with the original signal and degrades the visual quality of digital image. Different types of images consist of different types of noise [1,2] such as Rician noise, Quantum noise and speckle noise. Faulty instruments, data acquisition process, transmission and compression are some of the sources through which noise gets added into image.

Magnetic Resonance Imaging (MRI) is powerful diagnostic technique used in radiology. Magnetic Resonance Image (MRI) as the name suggest uses powerful magnetic fields and radio waves to capture structure of human body parts. MRI is often used to take images of the brain or other internal tissues, particularly when high resolution images are needed. MRI images with better resolutions have less Signal to noise ratio (SNR). Therefore, a proper denoising technique is necessary for improving image quality and higher SNR. The noise in MRI signal is a white Gaussian noise added to each part of the complex data. The magnitude image computed as the square root of two squared Gaussian variables added together has Rician distribution. This distribution becomes Gaussian in low SNR (background) area and Rayleigh in high SNR areas of the image.

Denoising of MRI images has been refined over a period with different algorithms and different assumptions, which has its own positive and negative results. Karl Krissian et al. proposed Noise-driven anisotropic diffusion filtering of MRI to reduce the blurring effect [3]. Buades et al. [4] proposed the nonlocal means (NLM) filter. NLM uses the concept of self-similarity. Yu and Zhao [6] proposed an efficient denoising process based on wavelet shrinkage for magnetic resonance imaging. A new MRI denoising method based on sparseness and self-similarity presented in [7]. Denoising of MRI images using fast NLM [8] was designed and Implemented on FPGA Platform.

In this paper, we propose BM3D algorithm for real-time processing on FPGA based on previous study of [9,10]. BM3D is an improved version of Non-Local Mean filtering. BM3D algorithm is a 3 steps process consists of 3D transformation of a group, shrinkage of transform spectrum and inverse 3D transformation. The algorithm performs grouping by block-matching, and by shrinking in a 3-D transform domain it achieves the collaborative filtering [11,12,13]. The objective of BM3D is to denoise the 3-dimensional stacks of similar patches using Wiener filtering. Winer filtering gives input from first stage of Noise Invalidation Denoising [14] as estimated data. BM3D preprocessing image with variance stabilization transform which stabilizes the noise variance in the MR image [15]. The denoising method can reduce the noise in MRI images more effectively on hardware accelerator [16-22]. The proposed BM3D algorithm implemented on SPARTAN6 Field Programmable Gate Arrays by using Xilinx ISE and simulated in ModelSim.

II. PROPOSED BM3D-NIDE-VST METHOD

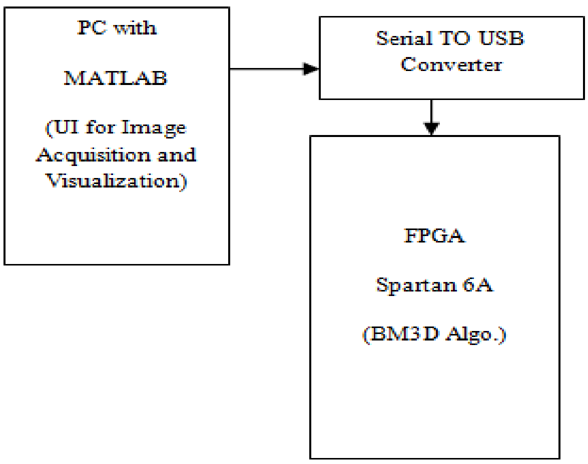

Figure1. System Block Diagram

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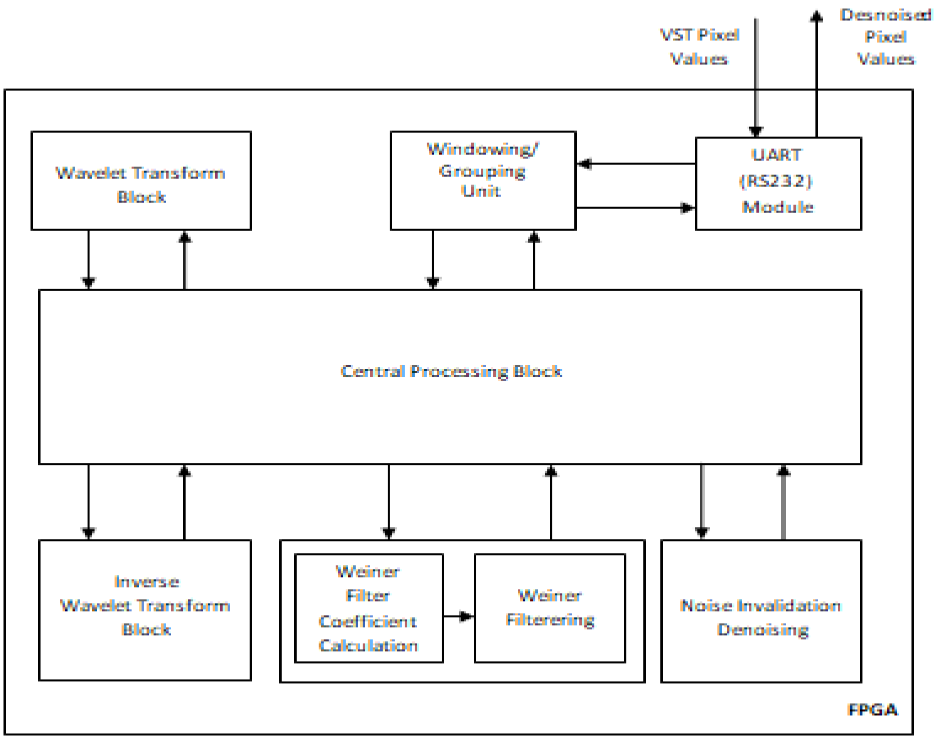

Figure2. FPGA Architecture of BM3D-NIDE-VST

Let $\bar{y}(x)|x \in \Omega$ be a 2D grey scale image defined in a spatial domain $\Omega \subset R^2$, where x is the coordinate of each pixel in the image. This image is corrupted with an additive Gaussian noise *w* which has a zero mean and variance σ2. The noisy image *y* can be representing as: $y(x) = \bar{y}(x) + w(x)$.The main goal denoising is to reduce the effects of $w(x)$ as much as possible [9].

Fig.1 shows system block diagram of the proposed algorithm. The main project is classified into two parts. In first part MATLAB graphical user interface allows the designer to open the image to be processed, setup the communication parameters, specify the required processing, send the input image, and receive the corresponding result after the process. After designing GUI, save this window by right clicking on each button choose view callback in that the MATLAB editor window will be displayed and corresponding code for respective button will be displayed. We can write the code in this window as per our requirement. In GUI simulation, we select COM9 port when we associate USB to serial converter, after that we check the association is open or close. Then we type the message and secret key and send the data.

In second part, FPGA using Xilinx platform studio (Spartan6 tool) is performing the task by receiving input pixels and apply BM3D denoising algorithm (implemented on FPGA) on it and send processed image samples to pc.

The architectural block diagram of BM3D-NIDe-VST algorithm is shown in fig 2. Working of each component is given below. MATLAB is responsible for creating the GUI and taking the input image from user, which is original MRI image. First convert original MRI image into grey scale image and for analysis performance of filter manually add % noise into this image. Before passing pixel values to FPGA board pre-processing input image using variance stabilization transform [10]. First, the noise variance is stabilized by applying a nonlinear variance-stabilizing transformation (VST) to the data. The resulting data can be treated as Gaussian with unitary variance, and thus, it can be denoised with any algorithm designed for the removal of Gaussian noise. In the final stage, by applying an inverse VST to the denoised data the desired estimate is obtained. VST processed pixels passing to FPGA board through serial communication. UART [RS232] protocol is used to exchange data from MATLAB to FPGA.

BM3D Denoising stage is made of two main filtering steps as NIDE and Wiener filtering. In both stages collaborative filtering is used. Collaborative filtering consists of four stages [8]: 1) Grouping patches similar to the reference patches. 2) 3D wavelet transformation of each stack of Patches. 3) Denoising wavelet coefficients (NIDe or Wiener Filtering). 4) Inverse 3D transformation.

In FPGA initially we are doing regrouping. First, we select one reference patch. According to this reference patch find out all the similar patches and club them together. In the same manner for different reference patches find out the different groups. In this way a group is a 3-D array formed by stacking similar 2-D patches together (image neighborhoods). After grouping perform 3D DWT and get wavelet coefficient.

In first stage of BM3D use Noise Invalidation Denoising (NIDe) instead of hard thresholding. In hard thresholding, threshold value is conventionally found and optimized based on a trial-and-error method on a dozen of samples whereas NIDE finds its optimum threshold based on the data and noise characteristics. The denoising procedure discards part of the signal that follows the statistics associated with the additive noise. After that apply inverse 3D DWT and we will get estimated image. This estimated image and VST processed image is used in the second step as input for wiener filtering. The above explained procedure will be repeated in second step as well. At the end of second stage, by applying inverse 3D DWT, we get denoised MR image. This denoised MRI image pixels transmit to pc. In Matlab inverse VST is applied on this denoised MR image to get final denoised MR image as output.

III. EXPERIMENTAL SETUP AND RESULTS

Field Programmable Gate Arrays (FPGA) generally described using Hardware Description Language (HDL). It is basically an array of programmable logic box. The architecture includes configurable logic blocks and I/O blocks and programmable interconnect. Clock circuitry will be used for driving the clock signals to each logic block. Multiplexers are used to route the logic within the block, to and from external resources and for clocked storage elements it contains flip-flops. To evaluate the performance of the proposed algorithm, we have implemented the design on Spartan 6 FPGA board. Mimas is an easy-to-use FPGA development board feature Xilinx XC6SLX9 TQG144 FPGA. Xilinx ISE 14.7 is used for synthesis and analysis of HDL designs. Xilinx ISE (version 14.7) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. In proposed algorithm Matlab2020a is used for image acquisition and visualization on graphical user interface. USB-to-UART Bridge Controller helps for updating RS-232 designs to USB using a minimum of components and PCB space. USB adapter is a type of protocol converter which is used for converting USB data signals to and from other communications standards. We use USB adaptors to convert USB data to standard serial port data and vice versa.

For testing T1, T2, and PD weighted MRI images of normal brain scan images have been used from the medical database available online. The parameters for proposed algorithm are chosen based on the optimized values proposed in [11] and are as follows: size of the patches k = 7, search window n = 17and image is resize to 64*64. Figure 3 shows the denoised results for T1 weighted MRI images when the noise level is 20%. For evaluation, table 1 show the PSNR and SSIM values of proposed method with Matlab implemented method. Figure 5 and 6 shows PSNR/SSIM vs noise leval comparision of BM3D-NID-VST (FPGA Vs Matlab).

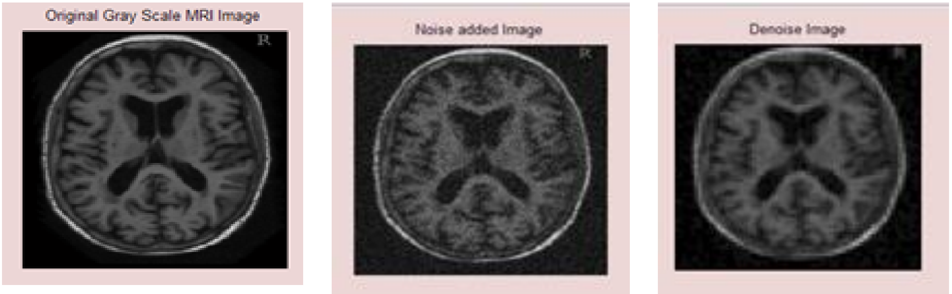

Figure 3. Original, noise added (20%) and de-noised image using FPGA

Table1. Quality metrics parameter comparison FPGA Vs MATLAB

Parameter Comparison of BM3D-NID-VST(FPGA VS Matlab)								
	Noise Level ->	**3**	**5**	**9**	**11**	**13**	**15**	**17**
PSNR	**FPGA**	33.08	30.01	26.36	25.06	23.94	22.97	22.08
	MATLAB	34.77	31.86	28.8	27.78	26.91	26.15	25.48
SSIM	**FPGA**	0.899	0.86	0.82	0.804	0.788	0.772	0.755
	MATLAB	0.93	0.89	0.81	0.77	0.74	0.71	0.69

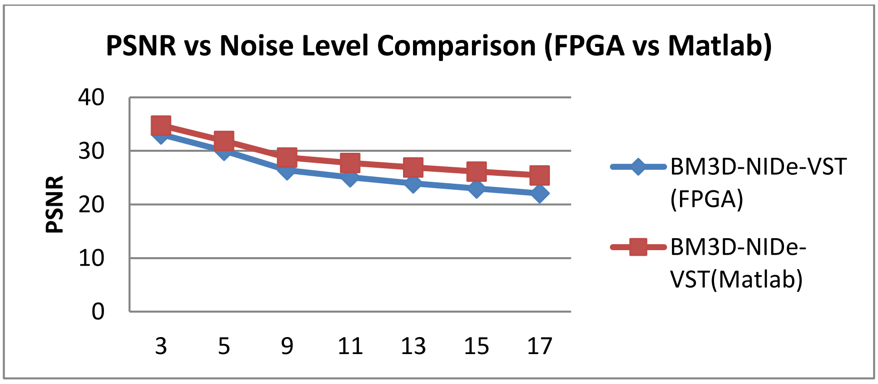

Figure 5 Graph: PSNR Vs Noise Level Comparison

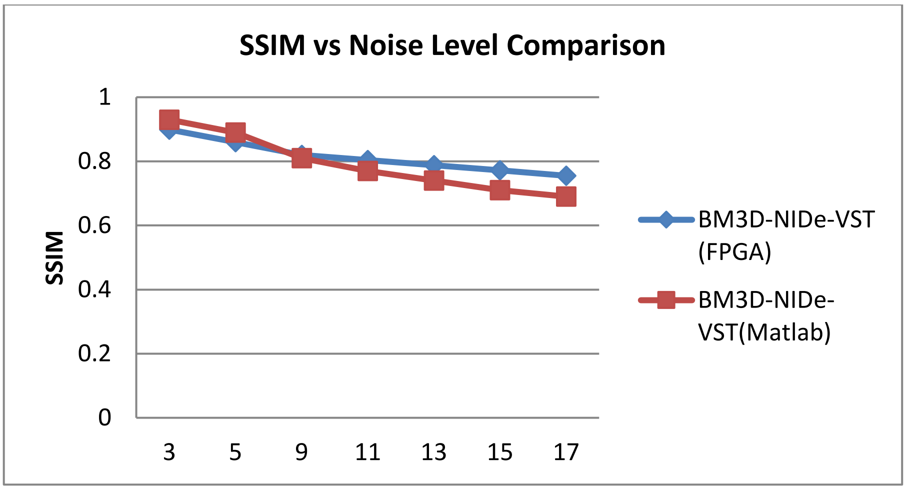

Figure 6 Graph: SSIM Vs Noise Level Comparison

Table2. Processing time on FPGA

Parameters	Time/Frequency
Minimum Period	4.658ns
Maximum Frequency	214.67 MHz
Minimum input arrival time before clock	4.590ns
Maximum output required time after clock	3.950ns

- **Calculating Block Processing Time**: Average Single Block Processing Time= 0.10 Sec (100 ms). Hence Total Processing Time= 409.6 Sec

- **Device Utilization**: FPGA has configurable hardware logic units; device utilization gives fare idea about no of logic units like FLIP-FLOP used in design.

Table3. Device Utilization Summery

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	74	11440	0%
Number of Slice LUTs	147	5720	2%
Number of fully used LUT-FF pairs	74	147	50%
Number of bonded IOBs	13	102	12%
Number of BUFG/BUFGCTRLs	2	16	12%

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I. CONCLUSION

In this paper, we propose an FPGA-based hardware accelerator for BM3D-NID-VST algorithm. This approach is shown in the MATLAB software as well as in Xilinx ISE design suite using VHDL code language. We have achieved significant improvement in processing time on FPGA compared to MATLAB without losing performance. Our results (PSNR and SSIM values) match with MATLAB results, there is no significant decrease in these performance parameters. By compromising little bit on performance parameters, we have gained huge improvement in processing time which makes this algorithm suitable for real time applications.

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