Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 12, Issue 07, June 2021: 14283-14296

Research Article

Wireless Sensor Network Radio System Structure and RF Implementation of Transceiver Circuit

Chandrasekhar Kandagatla [1], Dr. Prabhu G. Benakop [2]

[1] Associate Professor, Dept. of Electronics & Communication Engg., Aurora's Engineering College, Abids, Hyderabad
[2] Professor and Principal, Methodist College of Engineering and Technology, Abids, Hyderabad

ABSTRACT

In terms of overall system design, CMOS radio frequency (RF) transceiver architecture has a considerable influence. Performance, power consumption, die size and cost are the most important factors to consider while making a selection. The IEEE802.15.4 standard has a minimum performance requirement. According to the application in issue, all other considerations are of secondary importance. The RF transceiver must be able to interface with small devices, such as sensor nodes, in order to be portable and low-power. As a result of the battery's dimensions and kind, the system's size, weight, and cost are all determined by its power consumption. In wireless sensor networks operating in the sub-GHz ISM band, the design and testing of CMOS integrated RF transceivers is the emphasis of this chapter. Here, you'll learn about radio system design, RF transceiver circuits, and data collection. As a concluding illustration of the size and floor design of a high-integration transceiver device, we demonstrate a completely CMOS transceiver chip. This paper illustrates the wireless sensor network radio system structure and RF implementation of transceiver circuit.

Index Terms: CMOS radio frequency, CMOS transceiver chip, wireless sensor network radio system structure.

I. WIRELESS SENSOR NETWORKS CMOS RF

Due to the rising demand for wireless access, wireless communication has recently increased at an exponential pace. WSNs may be employed in the next generation of ubiquitous computing systems. For example, sensor networks may be utilised for environmental monitoring and surveillance, as well as in the military, health, and security sectors. In wireless sensor networks, power dissipation necessitates minimal power usage for a long time. Transceiver design for WSNs that is tiny, low-power, and low-cost has gained interest. The scaling of CMOS transistor technologies and the rising bandwidth accessible at ISM bands are two technical aspects that are driving the development of wireless technology. Most license-free channels need extensive RF transceiver design adjustments to handle both linear and nonlinear modulation[1]. Completely integrated wireless systems are difficult to manufacture on silicon-based substrates.

Design of The Transceiver

WSNs are low-power, short-range networks that can communicate over a small distance. WSNs are often dense networks that need low-cost nodes. The RF transceiver is the sensor node's most power-consuming and costly component in WSNS. Design approaches must change the cheap cost and low power requirements demands. Network communication protocols must be

established before deciding on a design strategy. Transmission quality is limited or unfettered by protocol and radio link specifications. The following are the most significant features of a receiver:

- Range of motion
- Sensitivity
- Linearity
- Figure of noise
- Noise in the phase
- Frequency of operation and band width
- Selectivity of channels
- Power consumption
- Effect of erroneous frequencies
- Effects of Leakage
- Rejection of the image band

The definition of dynamic range varies depending on the application. In detection systems, It's generally a combination of the transceiver's capabilities and the requirements of the system. such as BER1 and VER2. In low-performance transceivers, such as those used in WSN applications, dynamic range, linearity, and phase noise are less significant. The following are the key features of a transmitter:

- Efficiency in terms of power
- Capacity to manage power
- Signal power sent out
- Frequency of operation and band width
- Out-of-band emission is a type of emission that occurs when a signal is (ACI3, ACPR4)
- Products that use intermodulation (IMP)

Designers are compelled to utilise a certain transceiver because of the requirements in the transceiver standards. When the application and the designer's expertise are taken into consideration, the transceiver architecture and configuration may then be selected or constructed. In many radio link protocols, modulation technique has a substantial influence on transceiver design[2]. Signal quality is sacrificed to achieve a lower data rate., and spectral efficiency, simple transceiver designs may be used with basic modulations. A transceiver architecture and configuration will be selected, after which the necessary circuits and sub-blocks will be provided, followed by a performance study and optimization.

Heterodyne, low-IF, and zero-IF or direct conversion transceivers are often used in radio connections (DCR1 and DCT2). Each of these architectures has its own set of pros and limitations, thus the application's needs dictate which one the designer chooses. One of the techniques for short-range, low-power UWB applications is UWB impulse radio. Short, modulated pulses are broadcast from the antenna directly using this technique. This design does not support simple, narrow-band transceivers. The LNA-less wakeup receiver is another simple design that may be utilised WSNs.

II. LITERATURE REVIEW

Recurrence transceiver for multi-standard applications with high reconciliation and low IF is introduced by [5] with the aid of 130nm CMOS technology. Receiver, voltage-controlled transmitter, and power oscillator in quadrature phase make up the low-IF transceiver. (QVCO). A Capacitive Cross-Coupling (CCC) normal entry design and an I/Q demodulator are used in the low-noise driver stage. One of the suggested transmitters features a five-port transformer with

interchangeable capacitor banks and an I/Q modulator for reconfigurable output coordination of the radio frequency (RF) output. Receiver frequency ranges between 0 and 10 GHz and transmitter frequency ranges between 1.5-to-four-gigahertz. All of these technologies may benefit from the RF transceiver layout described here, including LTE, IoT, WSN, and more. Noise figure (NF) is near to 3 decibels (dB), the effectability of the collector is increased to 100.2 decibels (dBm), and the power gain is 15.4 decibels (dB). An output power of 23dBm, a PAE increase of 41%, a power gain of 25dB, and an ACPR equivalent of 31.8dBc are among the characteristics of the proposed transmitter. The recipient and transmitter have burn-throughs of 10.85 mW and 180.95 mW, respectively, that include the QVCO. A FoM (Foundation of Merit) of 191.5 dB and 2.45 dB is the total of the two numbers. Dynamic areas of 0.56 millimetres and 1.6 millimetres, respectively, are available for each of the proposed recipients and transmitters.

This study is co-authored by [8] Older adults may obtain a deeper grasp of human culture by observing others for a long time period. However, even if it can function for a long time without the aid of systems to maintain its battery capacity, it is difficult to get such a configuration. Monitoring of biosensor signals, which are referred to as MCU devices[3], which require a lot of power, is necessary in order to flag the biosensor for testing. Microcontroller unit function for extracting the unique advantages of bio signals should be replaced by low-power application-specific coordination circuit for biosensor highlight extraction. Wireless Body Sensor Networks (WBSNs) ASIC will be utilised as a clinical demonstration in this investigation. Low-power microcontroller (MCU), wireless semiconductor control, Power Management Unit (PMU), and low-power collecting limit are included in the wireless body sensor network. 90 and 45 nm CMOS technologies are employed in the suggested method. Results reveal that the conventional wireless body sensor network design at a comparable delay stood out from changes in vibration-resistant and decreased power consumption.

[9] have proposed an in-lodge radar application for a 24-GHz direct-change transmitter. An I/Q upshift blender, oscillator generator, and a power amplifier make up the transmitter's design. To improve the linearity of the I/Q upchange blender, a new transconductor is being introduced with a scratch-off IM3 third-request intermodulation contortion. For the I/Q LO generator's I/Q adjustment, a poly-stage channel, incorporating parasitic line inductance, has been proposed. The 24-GHz direct-change transmitter uses a very straight I/Q up-transformation blender and a fair I/Q LO generator to produce high linearity and I/Q adjusting characteristics. To put it simply, it's constructed using 65-nm CMOS technology and uses 150 mW of current. 8.6dBm at 24 to 24.5GHz and a picture dismissal ratio of 49.9dBc for the whole working band are the results of this device's overall performance.

[8] CMOS sliding-IF RF receivers for Bluetooth Low Energy (BLE) applications have been developed and are already available. All three of these components are incorporated in the LNA: the transconductance stage ($g m $), the IF blender, and the transimpedance intensifier (LO age block). IM2 bending was studied extensively in order to better understand how an OFDM blocker impacts the receiver's capacity to respond to a second-request intermodulation (IM2). To take use of the findings, an in-band two-tone blocker resistance measuring technique and an IM2 adjustment circuit have been developed. Debate on IM2 alignment and dc offset correction at the baseband enhancer stage may be settled more quickly if both issues are addressed at the same time. Body predisposition controls and door inclination controls are used to regulate the Dc offset and the IM2 alignment. CMOS-based 65-nm RF BLE RF beneficiary coordination circuit was created[4]. Attenuation level 10 dBm may be obtained utilising 3.55mW distributed from 1-V stock, which has an addition control range of +2 to +62 decibels (dB), as well as 3dB of base clamour figure. According to simulation results, the proposed IM2 alignment circuit may increase in-band two-tone blocker resilience by 7–12 dB. (2019) Short-range wireless sensor networks (WSNs) need low-power transceivers, and the 0.18 m 1-poly-6 metal CMOS innovation with 950 m 800 m operating range was chosen (902-926 MHz). The proposed WSN transceiver relies on a more refined iteration of the Amplitude-Shift Keying communication technique and has a better

nonstop RF tweaked transmission waveform without the requirement for expensive modulator/demodulator circuitry. Circuit approaches to decrease power dispersion and boost energy efficiency have also been employed. 1.58 mW of power is dissipated by the WSN transceivers, while their productivity is 21 percent.

In their article published in 2020, Kim Jungah and Lee Yongho describe a low-power CMOS dynamic opposition capacitance (dynamic RC) complicated bandpass channel (BPF) with customizable addition, data transmission, focus recurrence, quality factor, and passband levelness. Passband gain may be successfully regulated by tinkering with two cross-coupling resistors independently in cross-coupled biquad structures. The biquad-based complex BPF offered for a fourth request was examined for a baseband simple processor with low transitional recurrence (low-IF). The baseband simple processor has three first-request variable-gain enhancers and two difficult biquad channels. It was built in 65nm CMOS and achieved a tuning range of 15.6 to 50.6 dB, transfer rates of 1.5–3.9MHz and 1.5–4.1MHz, and a pass band evenness of 1 to 1 dB. It attained picture dismissal proportions ranging from 40.3% to 53.3% across the whole adding range. It used 1.4 mA from a 1 V supply and took up 0.19 mm2 of silicon substrate space. The proposed BPF system had the potential to increase sign preparation demonstrates via a pass band evenness that was flexible and wide-ranging in tenability, as well as an improvement in transfer speed, focus recurrence, and quality factor.

III. WIRELESS SENSOR NETWORK RADIO SYSTEM STRUCTURE

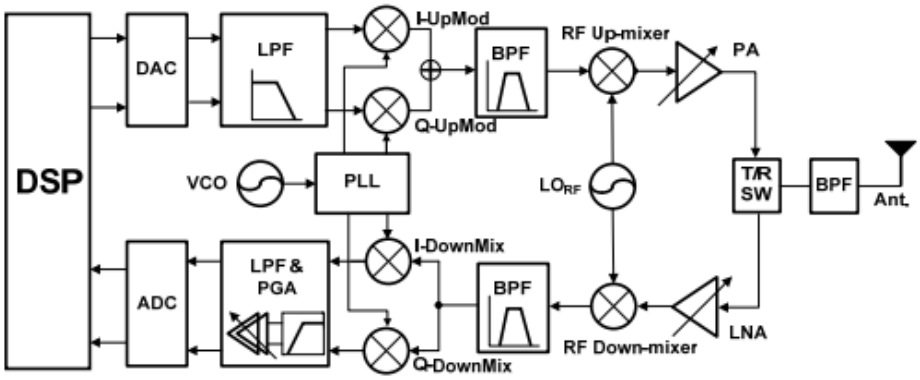
For example, heterodyne and zero-IF (intermediate frequency) transceiver designs exist, each with its own set of advantages and drawbacks; nevertheless, satisfying the needs of several applications while staying competitive becomes more challenging. Since it has been used for a long time and is well-known, the super-heterodyne design is the most common transceiver topology. In order to get the best results, it is the most popular architecture. As a result, it isn't ideal for fully integrated systems since it requires picture rejection and extra channel selection filters. The cost and power consumption of multi-band/multi-mode transceivers are additional concerns.

It is possible to achieve both high integration and low power consumption using low-IF and zero-IF architectures. For this reason, the concept of low-IF was coined: following quadrature conversion, both low frequencies include all the information required to distinguish between one another. With this technology, a DC offset is prevented, along with the usage of SAW filters and image RF filters. Even-order nonlinearity, LO pulling/leakage, and I/Q mismatch are a few of its flaws. Certain image rejection calibration techniques need a higher level of complexity and power consumption.

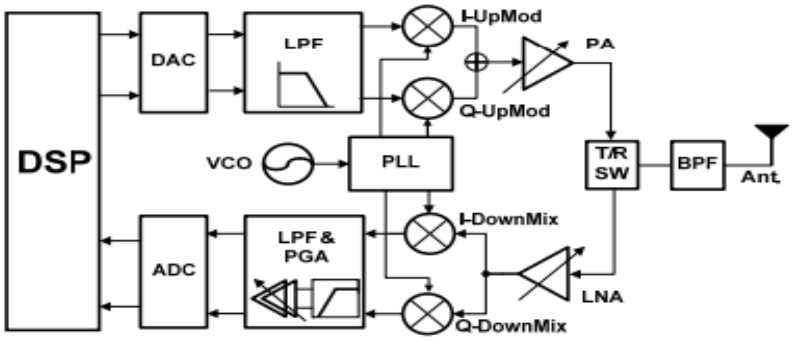
The zero-IF architecture is then used to do a direct baseband down conversion to the desired frequency. As a result, the frequency of the mirror signal matches that of the original[5]. This does not exclude the possibility that the zero-IF receiver has an issue with a reflected signal. For optimum integration, minimal power consumption, and cheap prices, it's still the best option. Besides that, it removes the requirement for a user to reject a picture. The LO frequency design to avoid LO pulling/leakage, DC offset issues, and flicker noise may not be the ideal solution for everyone.

All of a network's communication nodes must be constructed on the same chip in order to save power consumption and maintain wireless sensor networks affordable. Here is a visual representation of the WPAN system's structure. IEEE 802.15.14's physical and medium access control layers are supported by the RF transceiver and digital baseband processor. An on-chip voltage-controlled oscillator for frequency synthesis is shown in Figure (right) (VCO). This transceiver chip has an I/Q ADC and a 6-bit DAC for each of the two digital-to-analog converters (ADCs). In order to save energy, money, and space, the receiver has a zero-IF design.

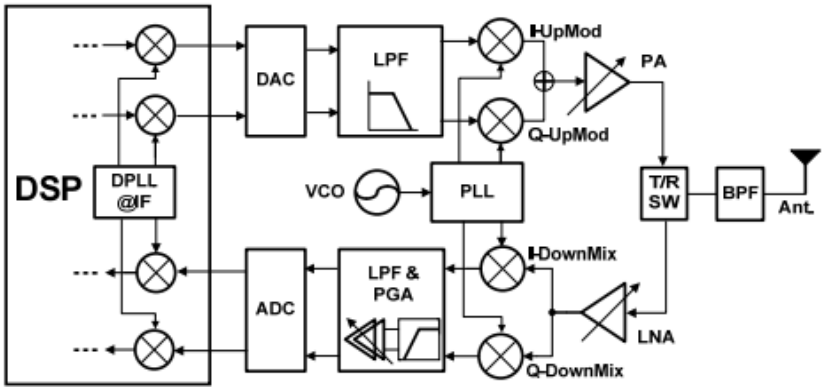
The image depicts the receiver's RF front-end circuitry. A low-noise amplifier is used to convert the sub-GHz RF signal to zero-IF I/Q signals from quadrature LO signals from a frequency synthesiser (LNA).



(a) Super-heterodyne architecture



(b) Zero-IF architecture



(c) Low-IF architecture

Figure 1 (a), (b) & (c) Transceiver architectures

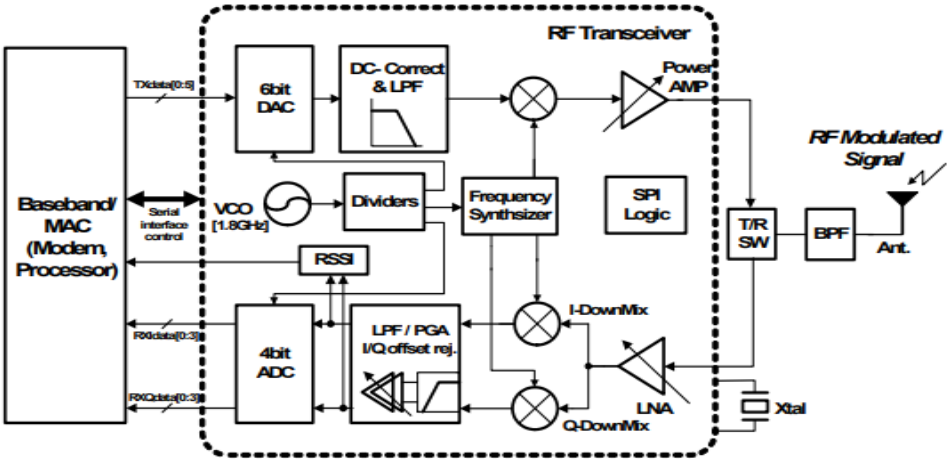


Figure 2: Wireless sensor networks in the sub-GHz ISM band are supported by the following system architecture: RF transceiver and baseband processor.

As part of the analogue baseband filtering and signal-amplification, a programmable gain amplifier and a third-order RC filter are utilised. The MODEM block's interface also includes I/Q 4-bit dual flash-ADCs. For current mixing, the transmitter uses an up-conversion mixer. Following a 6-bit DAC, the MODEM block's digital modulator produces baseband BPSK signals[6]. An RCP low-pass filter is used to combine baseband and 900 MHz signals. A high-efficiency nonlinear power amplifier may be used for high-power emission since BPSK modulation is constant envelop modulation. 900 MHz signals are generated using an integer-N frequency synthesiser and a 30 MHz crystal oscillator with 30-ppm accuracy. The 1.8 GHz LO signals are generated using an on-chip inductor with a high Q (quality factor). The LO I/Q signals at 900 MHz are then divided in half for use in both TX and RX mode frequency mixing. Common mode noise immunity is achieved by constructing the frequency synthesiser as a differential circuit.

For WSN applications, RF transceiver ICs' power consumption must be carefully considered. Compromises in system power consumption, gain, noise figure, chip size, and linearity are required to accomplish this. It is possible to minimise battery leakage current and sleep mode current by optimising current sources in WSN applications. Sleep mode current can be reduced even if system IC performance decreases by using tiny devices with limited active area. An on-chip inductor may reduce power consumption in driving pads and trace parasitic capacitances.

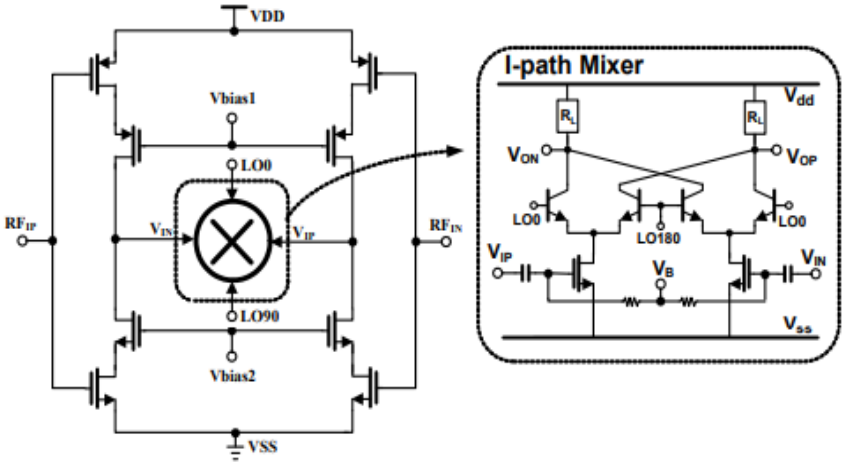


Figure 3: Input/output (I/Q) converter mixer RF front end of receiver: low noise amplifier

A low-power current mixing approach and a resistive load may be used to create a transmit RF front-end that consumes minimum power due to a relatively low transmit power of -3 dBm.

IV. RF TRANSCEIVER CIRCUIT IMPLEMENTATION

The RF transceiver chip contains six metal layers and a 2-micron thick top metal, and it is just 0.18 microns thick. RF and analogue circuits benefit from this technology because the on-chip inductor has a high gain and a high quality factor (Q) (8).

Receiver

The RFE of a working WPAN receiver chain is made up of LNAs and quadrature mixers. Using current-reuse complementing techniques, a balanced sub-GHz LNA may be produced without the need for a huge inductor. It is done externally using passive LC components to match the inputs. An IIP3 of 5.2 decibels is achieved at maximum power, with a noise figure (NF) of 2.6 decibels. Using Gilbert-cell quadrature frequency demodulation, a single analogue baseband channel is created from the LNA's differential outputs. Vertical bipolar transistors in the switching quadrant of a direct-conversion receiver help to minimise mixer gain due to reduced 1/f noise. The Gilbert multiplier type with source-grounded design has a wider voltage range, which provides more linearity. 6 dBm is predicted for IIP3. The implemented WPAN receiver's analogue front-end (AFE) is made up of the Filter Tuning Circuit, and DC Offset Cancellation Block (AFE).

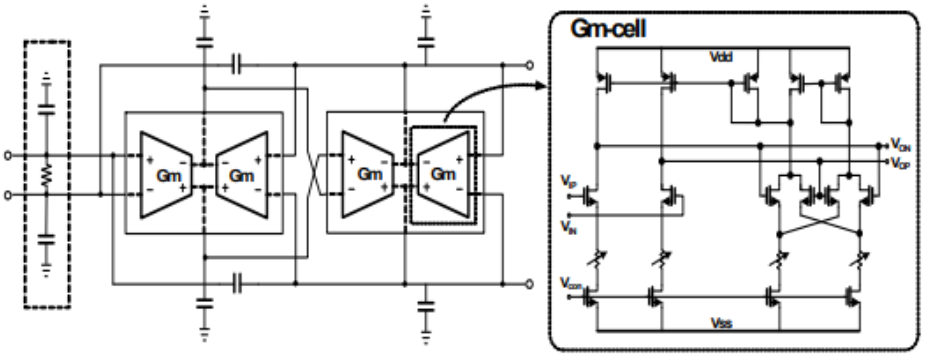


Figure 4: Channel selection filter using third-order Butterworth LPF employing suggested trans conductance cells in receiver I's analogue baseband circuits (Gm-cell)

To increase the Butterworth filter's third-order dynamic range, a programmable gain cell was sandwiched between a cascading biquad and single pole cell. The AFE's design focuses on lowering the die size in order to maximise dynamic range while minimising power consumption. Baseband noise is heavily influenced by thermal noise generated at the quadrature mixer outputs by PMOS current sources. In order to increase matching and reduce flicker noise, all transistors have long channel lengths. To ensure that the receiver's dynamic range is not limited by the built-in DC offsets, a baseband modem control signal is required. In contrast to other routes, the target band is able to pass through.

Due to the fact that it is a DCR structure, 1/f noise and DC offset must be eliminated. Initial filtering ensures that the filter can meet PGA and ADC SFDR specifications. Figure 4 shows a third-order Butterworth LPF. Biquad overshoot compensates for in-band loss while passive single-pole resistors at the mixer's output stage reduce interference that might impair the dynamic range of baseband inputs. With a degeneration resistor, a Gm-cell is shown in Figure 4. In order to save space, two Gm-cells are joined into one for LPF. The cell's lumped resistor and MOS size must be correctly calibrated in order to enhance the Gm-linearity. If you're going to get the most out of your RF input signal, you'll need a dynamic range of at least 78%. Received from the

baseband modem is a digital control signal that is sent to the automated gain-control (AGC) signal. In this receiver's PGA, each of the three gain stages is capable of raising gain by 1 dB from 0 to 65 dB. In order to maintain the PGA's linearity, the resistor switching method was used. Dedicated hardware was used to build a connection between the baseband modem block and the I/Q 4bit twin flash-ADCs

The receiver line's maximum DC current usage is roughly 6 mA.

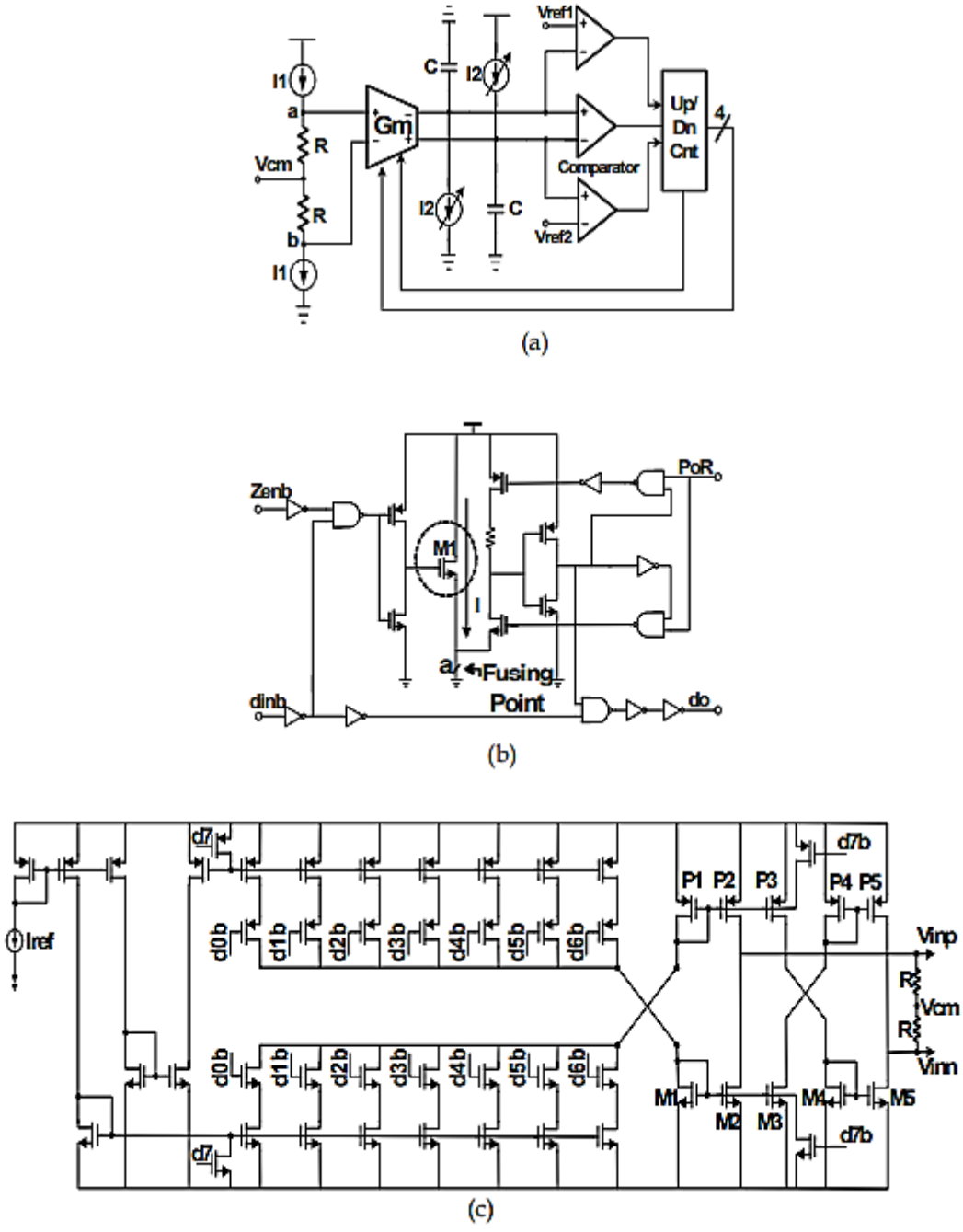


Figure 5: Analog baseband circuits of receiver II: (a) The tuning circuit for channel selection filter (b) The circuit of fusing cell for filter-tuning (c) DAC schematic for DC offset adjustment

The automatic-tuning circuit in Image employed an indirect tuning method, as indicated in the figure. A constant pole frequency is required because the trans conductance value influences Gm-C filter performance. No matter what occurs within or outside of this procedure, gm should stay constant. The output current-to-voltage ratio, the sinking or sourcing current, and the current needed for sinking or sourcing must all be kept constant in order to minimise gm fluctuations caused by bias block temperature changes (as illustrated in Figure). As demonstrated in Figure, the gm-input cell voltage stays constant even though the MOS bias component and the resistance temperature are both compensated for. Convergence time is less than 100 milliseconds for the tuning circuit Since the value of a parameter specified for the first time has an influence on gm, if the cut-off frequency deviates from the planned value, gm must be modified. When SPI is implemented, the value of the fusing is set in stone and cannot be changed.

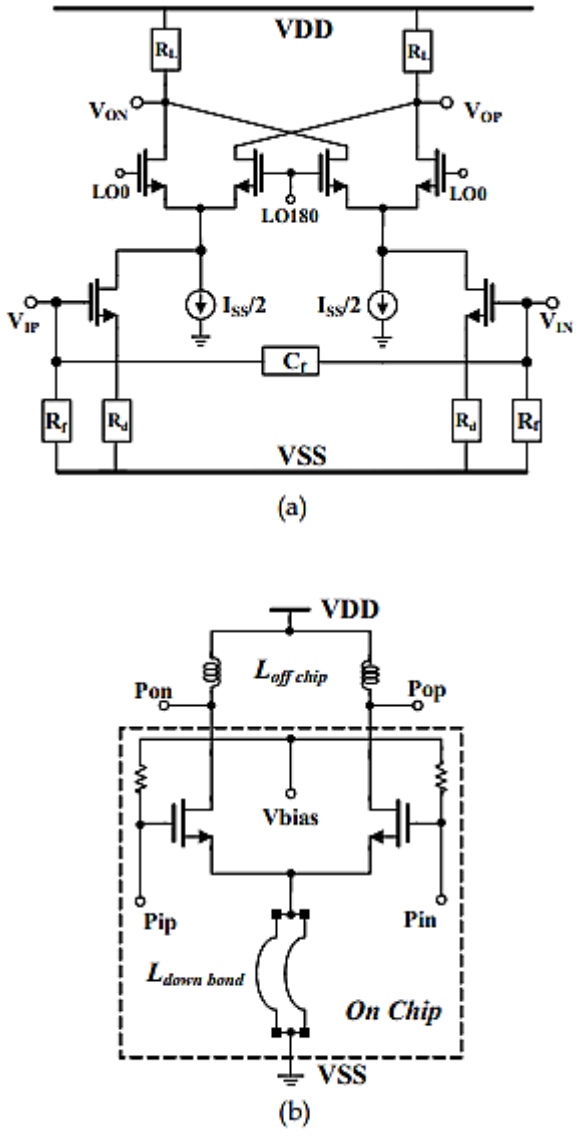


Figure 6: Transmitter circuits: (a) an up-conversion I/Q modulator (b) Off-chip inductor drive amplifier

This schematic depicts the circuit needed to fuse a cell (b). At starting, the low PoR signal voltage is amplified within the amplifier's range, which is adjusted to a ratio of their PMOS channel resistance to NMOS channel resistance. Inverting amplifier latches on to the high PoR signal and it does not change during normal operation ZENB and DINB are both SPI signals that may be

used to enable or disable a device. A "power on reset" (POR) enable signal, as opposed to a "fusing cell output signal" (FIP). When the fusing signal is activated, the output signal from the fusing cell is always the same. Current capacity M1 must exceed 1 milliamperes in order to remove the fused point while still providing the enable signal to other components. Negative DC offsets must be eliminated from PGA1 and any feedback loop used to lower LPF output offset must be minimised for correcting DC offsets. According to Figure 6(c), 8-bit input data is converted into the PGA output voltage by means of an 8-bit DAC. LPF output has a 640 mV DC offset and a 5-mV precision for a single bit change. As a current mirror for the DAC, the MOS (P1P5, M1M5) must be big enough to compensate for the imbalance. The MOS's 20m/2m aspect ratio is put to excellent advantage in this application.

Wireless Transmitter

The transmitter route must undergo a digital-to-analog conversion in order to transmit the BPSK modulated baseband signal. The illustration depicts a mixer with an RC low-pass filter. A second RC low-pass filter utilises a current mixing approach to filter baseband analogue signals before they are converted to RF frequency. Current mixing reduces the need for linear modulator inputs when creating a high voltage-driven DAC output signal. Additionally, the modulation quality of this frequency-up modulation technique is likely to be quite high.

power consumption, and linearity.

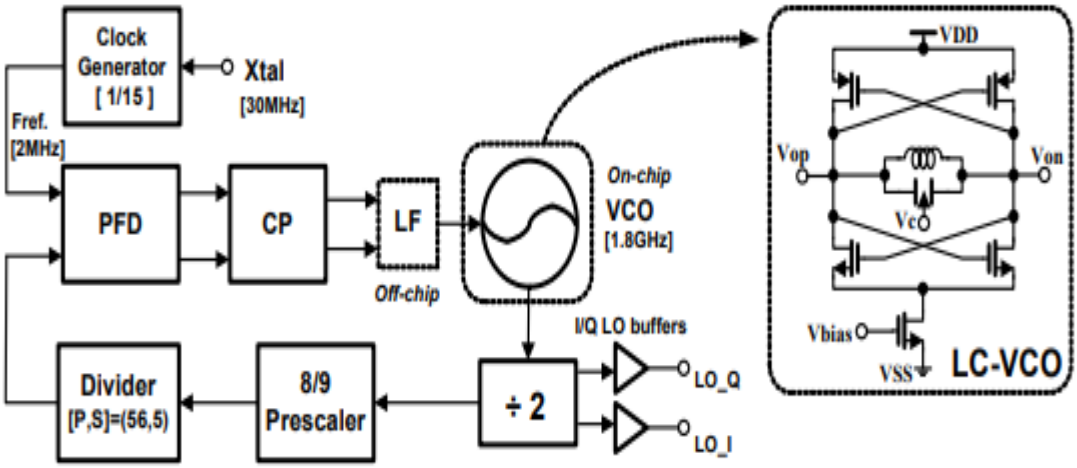


Figure 7: Voltage-controlled oscillator frequency synthesiser block diagram

Using a -20 dBm differential signal, the balanced mixer can transform baseband transmissions up to 900 MHz and transmit it to the power amplifier. For example, spectrum regrowth is caused by the Gilbert cell nonlinearity and quadrature imbalance in the modulator circuit quadrature mismatch. As a result of careful design, extra antennas are not required since the LO emission and spectrum redistribution are reduced. This differential common source design employs a high-Q off-chip inductor as the driver amplifier. Using many down-bond wire inductors reduces spectrum regrowth. A complete transmitter path uses 7 mA of simulated DC current. A 3.3 Hz frequency synthesiser The transmit/receive LO signal is generated using an Integer-N frequency synthesiser with a second-order passive loop filter. It is necessary to split a 30 MHz crystal as an internal reference. 900 MHz low-noise (LO) signals may be generated using voltage regulated oscillators (VCOs). Resonator components include a four-turn spiral inductors and a varactor. The nMOS/pMOS complementary architecture of the Negative-Gm core cell delivers excellent power efficiency and gain.

Synthesizer of Frequency

The LO signal is generated using an Integer-N frequency synthesiser with a second-order passive loop filter. Internally, a 30 MHz crystal reference is split. As indicated in Figure, the VCO used to produce the 900 MHz LO signals is a 1.8 GHz voltage controlled oscillator (VCO). A varactor and a four-turn spiral inductor make up the LC-resonator. The nMOS/pMOS complementary architecture of the Negative-Gm core cell delivers excellent power efficiency and gain.

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{LC_{eff}}} \qquad (1)$$

The equation for the VCO's oscillation frequency is shown here (1). Between 1.6 and 2.2 GHz, the VCO's tuning frequency may be simulated. With two latches, the high-frequency divider circuit has a negative-feedback design. Fast locking and excellent linearity of the phase transfer function are achieved by combining a D-flip-flop (DFF), an AND gate, and a delay time block. It is possible to decrease output switching noise and up/down current mismatch using a nMOS/pMOS cascade topology. An external 30-MHz crystal oscillator is used to generate the sample clocks for the ADC and DAC in the clock-producing block. A full frequency synthesiser route's simulated DC current usage is 8 mA.

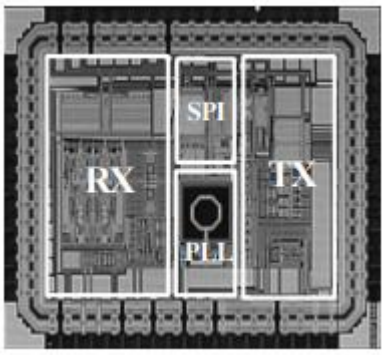


Figure 8: Die microphotograph

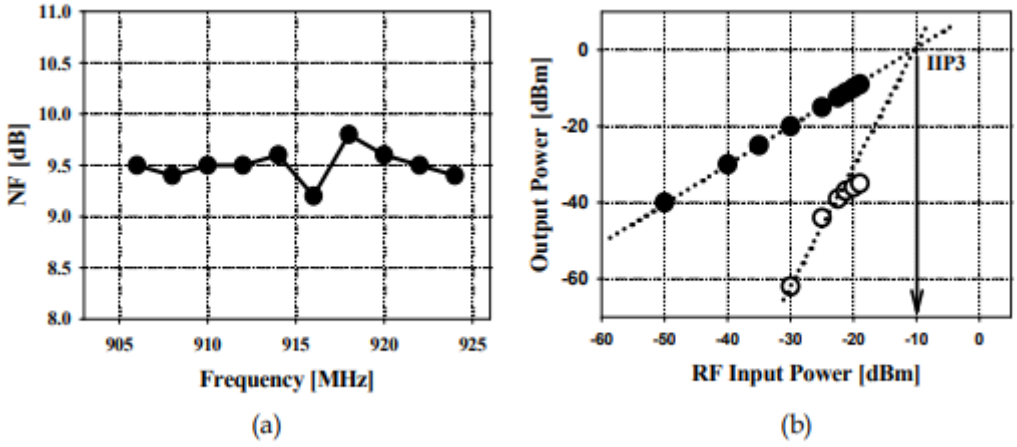


Figure 9: Measured results: (a) cascaded noise figure (NF), (b) cascaded IIP3 of overall receiver

V. WHY RF CMOS?

Can and can CMOS ever completely replace bipolar transistors in any analogue or RF application? Do we have to get rid of bipolar technology? These are the types of issues that have been discussed in a number of recent conferences [Gil98]. Bipolar supporters and CMOS advocates regularly engage in acrimonious debates on this issue. Concerns and disagreements about climate change are not going away anytime soon, and they need to be addressed.

Ease of Obtainment and Readiness

Of all semiconductor IC technologies, CMOS is the most commonly available and accessible. A wide range of CMOS processes are available from semiconductor foundries across the globe. CMOS is the technology of choice for the great majority of digital applications, which account for the vast majority of annual worldwide semiconductor sales. This means CMOS will continue to be the dominant technology in the future. In addition, this is the major advantage of the CMOS technology over Bipolar or BiCMOS, and is the origin of the phrase "RF CMOS." As a result, CMOS' dominance will also bring other advantages, such as access to the largest pool of technical resources and financial investment.

Profitability and Integration Efforts

One of the main advantages of CMOS technology, according to its advocates, is its lower cost and high degree of integration (number of transistors per square inch of silicon). In comparison to a technique that uses just majority carrier devices, the defect density of a bipolar transistor process is larger. Since the CMOS process will always create more chips, the cost per die will be reduced. Bipolar processes are becoming less common as a result of their low integration level. As a consequence, the cost of using a BiCMOS method to construct bipolar transistors is increased since more masks are required. In contrast, bipolar advocates tell us that the cost advantage of the CMOS technique may not be as considerable. While many RF or analogue chips are small, the costs of packaging and testing make the price of RF chips comparable to those of their analogue counterparts. If all of the digital chips are integrated in a wireless chipset, the cost advantage of RF CMOS may not be realised at all.

Furthermore, a pure digital process is not the same as an RF or analogue one. To make high-quality passive components like resistors, capacitors, and inductors, more masks are needed.. Masks' cost advantage to the CMOS industry may not be realised because of this. Another advantage of using a BJT is that it may be used in conjunction with a MOSFET, allowing for the integration of other circuits (such as a VCO) on the same chip or the realisation of lower-cost architectures (like direct conversion radio).

CMOS advocates argue that CMOS technology has no cost advantage over Bipolar or BiCMOS. All of this seems to back up their claims We believe that RF CMOS is more cost-effective than BiCMOS in terms of lithography node technology. Even so, this cost advantage may not be fully realised without additional masks related to high-quality passive components, such as in the case of Radio or System on Chip (RoC or SoC) where wafer cost is a large portion of total system cost; unless the RF transceiver can be designed in a pure low-cost digital CMOS process without the need for additional masks, such as in the case of Radio or System on Chip (RoC).

VI. CONCLUSION

In RF and analogue applications, bipolar transistors have undeniable performance benefits over MOSFETs. Here are a few examples:

- A high gm/I ratio, which is crucial for parameters like as gain and power consumption; (the gm/I of a MOSFET will never be higher than that of a bipolar transistor [AboOO].)
- Bipolar transistors provide better device matching on the same chip than MOSFETs; low 1/f noise is essential in oscillator design and low jitter applications.
- Bipolar transistors have analogue properties that are exact, therefore highly predictable [Gil98], and readily modelled, as opposed to hard-to-model deep sub-micron CMOS transistor behaviour. Model parameters in modern BJT devices are less than thirty, but model parameters in deep sub-micron CMOS devices are in the hundreds, and each MOS shape requires a separate model. Even yet, RF CMOS modeling fails to forecast impedance and noise figure accurately;

Due to hot carrier deterioration [LiqOl], bipolar transistors may operate at greater voltages than MOSFETs without affecting reliability. Voltage Vce between the collector and emitter in RF bipolar transistors may exceed the supply voltage. Deep sub-micron MOSFETs may need biassing the drain-source voltage Vds much below VDD for analogue applications. An 18 p,m gate MOSFET with a Vds = VDD bias will last fewer than ten years, even when it is at saturation. A 10-year lifetime for digital circuits may be achieved by using the same VDD for transistors. When the switches are transitioning, they are only saturated for a fraction of a clock cycle. It may be necessary for CMOS circuits to operate at lower voltages than their bipolar counterparts, which may result in a smaller head or leg space. MOSFETs, on the other hand, are better in every manner than bipolar transistors. CMOS transistors provide a variety of interesting advantages in terms of performance. One of them is linearity [Gil98]. Because of their greater linearity, SiGe BJTs outperform Si BJTs. The exponential I-V law has a detrimental effect on transistors in low-distortion, medium/large signal applications. Because the signals have already been amplified by the previous LNA, this is extremely important in mixer design.

High IP3 may be achieved in bipolar transistors by using a large amount of emitter degradation. Additionally, inductive degeneration requires a huge silicon surface, whereas resistive degeneration, although needing a smaller silicon size, adds extra noise and decreases legroom. Another advantage of CMOS is that a pMOS chip may be used in conjunction with it. None of it has been tested for its RF/IF implementations. CMOS still offers a few, if not many, performance benefits over pure bipolar technology, despite the fact that it is more expensive. This paper illustrated the wireless sensor network radio system structure and RF implementation of transceiver circuit.

REFERENCES

1. *Nasri, Mohen. (2012). A 2.4-GHz-Low-Power CMOS RF Transmitter for IEEE 802.15.4 Standard. Wireless Sensor Network. 04. 173-176. 10.4236/wsn.2012.46025.*

2. *National Coalition on Health Care. in http://www.nchc.org/facts/cost.shtml*

3. *Mohammed Sulaiman BenSaleh, Raoudha Saida, Yessine Hadj Kacem, Mohamed Abid, "Wireless Sensor Network Design Methodologies: A Survey", Journal of Sensors, vol. 2020, Article ID 9592836, 13 pages, 2020. https://doi.org/10.1155/2020/9592836*

4. *Lee, Ho-Yin & Chen, Shih Lun & Chen, Chiung-An & Huang, Hong-Yi & Luo, Ching-Hsing. (2007). Wireless Thermal Sensor Network with Adaptive Low Power Design. Conference proceedings : ... Annual International Conference of the IEEE Engineering in Medicine and Biology Society. IEEE Engineering in Medicine and Biology Society. Conference. 2007. 5891-4. 10.1109/IEMBS.2007.4353688.*

5. *S Sarkar P. Sen, A, Raghavan, S.Chakarborty, and J.Laskar, "Development of 2.4GHzRF Transceiver front-end chipset in 0.25µm CMOS," in Proc. 16th inst. Conf. VLSI Design 2003, pp. 42-47*

6. *Xu, Yongzhao & Hu, Xiduo & Kundu, Sudip & Nag, Anindya & Afsarimanesh, Nasrin & Sapra, Samta & Mukhopadhyay, S.C. & Han, Tao. (2019). Silicon-Based Sensors for Biomedical Applications: A Review. Sensors. 19. 2908. 10.3390/s19132908.*

7. *Zubiete, Enrique & Fernandez-Luque, Luis & Medina, Veronica & Gomez Gonzalez, Isabel Maria. (2011). Review of wireless sensors networks in health applications. Conference proceedings : ... Annual International Conference of the IEEE Engineering in Medicine and Biology Society. IEEE Engineering in Medicine and Biology Society. Conference. 2011. 1789-93. 10.1109/IEMBS.2011.6090510.*

8. *Fouad, Mohamed & El-Bendary, Nashwa & Ramadan, Rabie & Hassanien, Aboul Ella. (2013). Wireless Sensor Networks, A Medical Perspective.*

9. *Deen, M.J. & Murji, R. & Fakhr, A. & Jafferali, N. & Ngan, W.L.. (2005). Low-power CMOS integrated circuits for radio frequency applications. Circuits, Devices and Systems, IEE Proceedings -. 152. 509 - 522. 10.1049/ip-cds:20045069.*