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Research Article

# Evaluate of Stand by Leakage current in CMOS Circuits by Sleepy methodology

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## ABSTRACT

**In the CMOS based VLSI circuits technology scaling is done towards down due to its size and for achieving higher operating speed. As we know that leakage power consumption of current in CMOS technology is a great challenge. We have also considered size, leakage power, average power & speed of operation (delay) in such a way so that we can control the leakage current. The sub threshold voltage is declining in successive nanometer technologies and has an associated effect of enhanced leakage current. We have also studied previous techniques in which the leakage power increases in an integrated circuit. Because transistors leak even when they are not activated and significant power dissipation takes place even during inactive state of circuits. The sleepy technique provides maximum leakage current reduction with lower output levels. The proposed circuit technique has been applied to some inverters and the result has been compared with earlier inverter leakage minimization techniques. All low leakage models of inverters are designed and simulated in Tanner Tool technology.**

***Index Terms*-- Average power, Leakage power, sleep transistor.**

## I. INTRODUCTION

IN CMOS digital circuit power dissipation consists of static and dynamic component. As we reduce size of digital circuit for achieving high operating speed result in increased sub threshold leakage current through a transistor when it is off. Other region for leakage is that transistor not off, that means some leakage occurs .There are several VLSI techniques to reduce leakage power[1].

For a CMOS circuit the power dissipation occurs during the active mode of operation due to dynamic and static components but in the standby mode, the power dissipation is due to the standby leakage current. In the hand held devices based on nanometer technologies static power consumption is a prime concern. Due to down scaling in the size down along with the improvement in operating speeds of CMOS VLSI circuits; the leakage power is increased with the growth of technology [5] .

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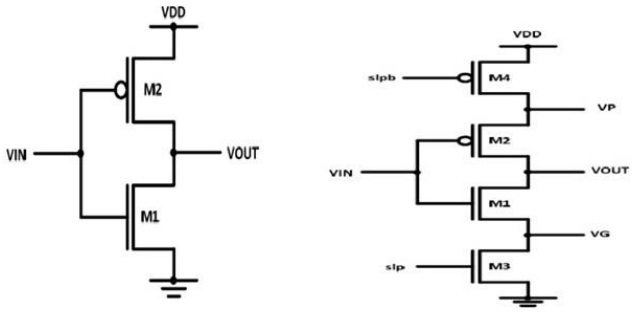
The sub threshold voltage is declining in successive nanometer technologies and has an associated effect of enhanced leakage current.

For successive technology generations the transistor feature sizes are becoming smaller and the channel length is reducing. The threshold voltage and gate oxide thickness are also being scaled down to maintain performance. We have also studied previous techniques.

The sub threshold voltage is going down to keep pace with reduced supply voltage for scaled down technologies in order to have good performance. The lower sub threshold voltage in nanometer technologies gives rise to enhanced leakage current because transistors cannot be switched off completely. Sub threshold current is the drain to source leakage current when the transistor is off. Thus it is essential to reduce leakage (static) power consumption during the idle or standby states of the circuits [2].

When a CMOS circuit is active, the total power dissipation is due to dynamic and static components. In the inactive (standby) mode, the CMOS circuit dissipates power due to the standby leakage current.

In sleep transistor technique (gated-VDD and gated-GND) technique, pull-up and/or pull-down or both networks are cut off from supply voltage or ground using sleep transistors (figure 1). This approach provides very good leakage power reduction but loses the state information when it enters in to sleep mode. Sleepy Keeper approach introduces additional keeper transistors to the sleep transistor technique to retain the state of the circuit.




**Normal Inverter** **Sleepy Inverter**

**Figure: 1 Diagram for a normal inverter and sleep inverter**

For a turned off single transistor leakage current ($I_{sub0}$) can be expressed as follows.

$$I_{sub0} = Ae^{\frac{1}{nV_e}(V_{gs0} - V_{th0} - \gamma V_{sb0} + \eta V_{ds0})}(1 - e^{-V_{ds0}/V_e}) \quad (1)$$

$$= Ae^{\frac{1}{nV_e}(-V_{th0} + \eta V_{dd})} \quad (2)$$

Where, $A = \mu_0 C_{0x}(W/L_{eff}) V^2_\theta e^{1.8}$; n is the sub threshold swing coefficient and $V_\theta$ is the thermal voltage $V_{gs0}$ , $V_{th0}$, $V_{sb0}$ and $V_{db0}$ are the gate-to-source voltage , the zero-bias threshold voltage the base-to-source voltage and the drain-to-source voltage , respectively ,γ is the body bise effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient, μ is zero bise mobility, $C_{ox}$ is the gate-oxide capacitance, W is the width of transistor , and $L_{eff}$ is the effective channel length[1].

All these techniques are applied to NAND and NOR gates and their functionality as well as power dissipation performance both in static active mode, sleep mode of operation are experimentally analysed in tanner tool.

## II Estimation of Leakage current in Sleepy technique

The sleep transistor is turned on during active mode of operation and turned off during idle or standby mode of operation. When the sleep transistor is off the virtual ground terminal VG will be at a nonzero potential. The gate to source voltage of off transistor becomes negative and its threshold voltage increases. This has an effect of reducing sub threshold current flowing between drain and source of the transistor. The substrate to source voltage and drain to source voltage also reduce and give rise to higher threshold voltage. All these effects cumulatively add up to lowered sub threshold current that flows in the off transistors. In this work we have proposed sleepy techniques for reduction of leakage current in inverters with and without application of state retention property. We have used these techniques for the reduction of power dissipation during inactive (standby) mode of operation. The reduced power is compared to traditional power gating methods for circuit techniques. As we have discussed before that in CMOS circuit power dissipation occurs due to dynamic and static components during the active mode of operation and standby condition the power dissipation is by the standby leakage current. Now I will improve the leakage current by using tanner tool and the transient analysis from range 90nm to 45 nm. So we compare all the result and I will improve some leakage power as compare pervious work to achieve better performance.

## III SLEEPY (NAND & NOR)

### 3.1 Sleepy NAND

The Sleepy NAND GATE technique for low leakage operation of an inverter is shown in below figure 2. This inverter though provides significantly leakage power reduction

In figure 2. shows Sleepy NAND for during operation As was expected, the sleepy technique shows lower power consumption for the NAND gate design with respect to the conventional design. The reduction in power is more significant for the standby mode, which appreciates the effectiveness of the design for the lower leakage power.

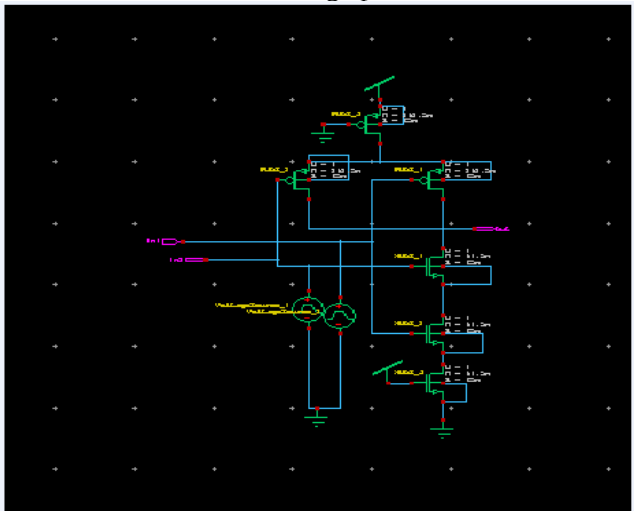


**Figure: 2 Sleepy NAND inverter**

### 3.2 Sleepy NOR:

The SLEEPY NOR gate for low leakage operation of an inverter is shown in below figure 3. This inverter though provides significantly leakage power reduction.

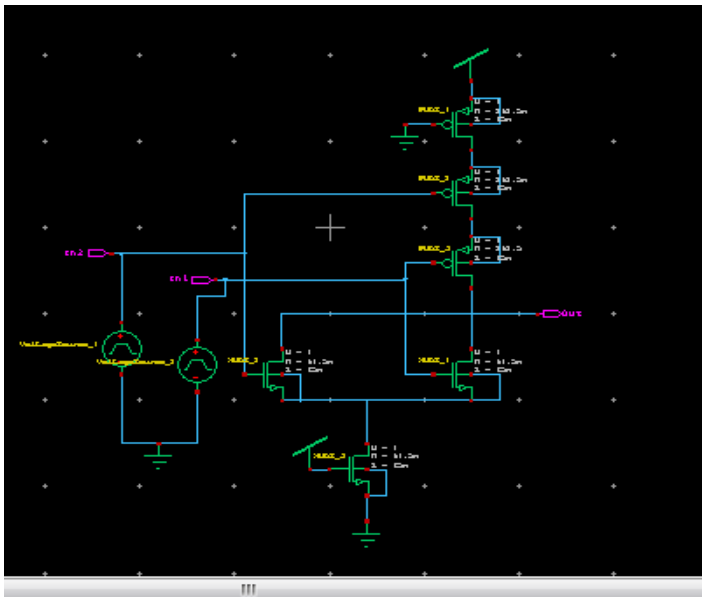


**Figure : 3 Sleepy NOR inverter**

Figure 3 shows Sleepy NOR for operation the sleepy NOR inverter signal is held at logic 1 voltage level and find the average power.

## IV. Novel Sleepy Technique (NAND and NOR)

### 4.1 Novel sleepy NAND

The Novel SLEEPY NAND Inverter technique for low leakage operation of an inverter is depicted in below figure. This inverter though provides significantly leakage power reduction.

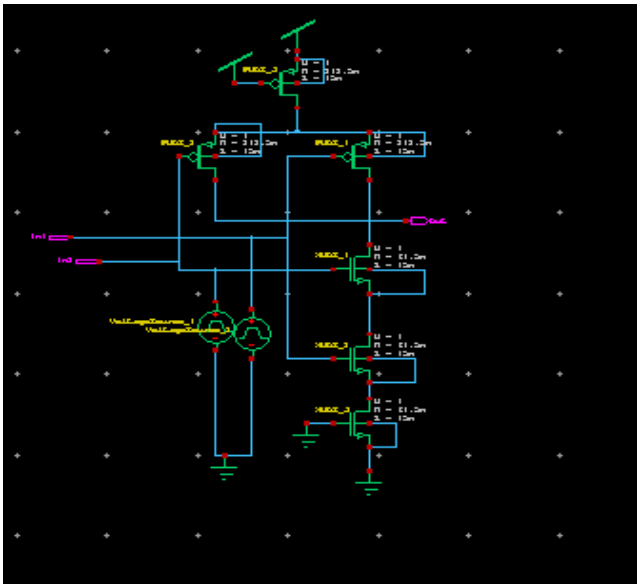


**Figure 4: Novel Sleepy NAND Inverter**

Figure 4shows Novel Sleepy NAND gate for during operation the sleep signal both held at logic 11 voltage level. This inverter though provides significantly leakage power reduction.

### 4.1 Novel sleepy NOR

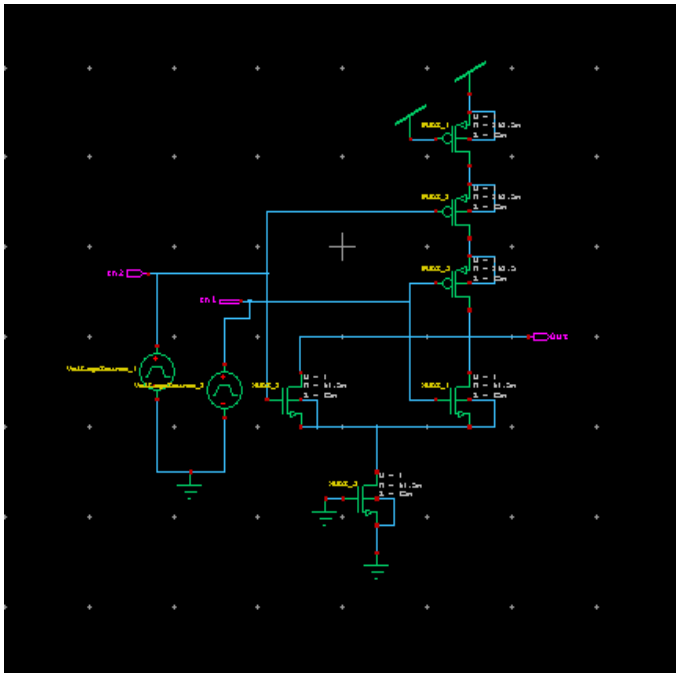


**Figure :5 Novel sleepy NOR inverter**

Similarly novel sleepy Nor gate for low leakage operation of an inverter is shown in figure 5. This inverter also provides significant leakage power reduction.

## V. SIMULATION AND RESULTS

The circuit design is carried out using 65 nm and 45n CMOS NAND and NOR Gate technology files. Table I & II provides Total power dissipation during pulsed operation for two input NAND and NOR gates. All the designs are done and simulation is performed in Tanner design environment. The total (average) power dissipation is measured using Tanner tools. All the gates are controlled by the sleep signals of same pulse width and period for the sake of comparison. The CMOS NAND and NOR Gate using sleepy, novel technique has exhibited lower leakage current and lower power. The average power dissipation during sleep operating modes is measured by using Tanner result browser and calculator.

***I. In Table CMOS Sleepy NAND and NOVEL Sleepy NAND Gate total (Average) power***

| S.no | Gate | Power(watt) at 65n | Power(watt) at 45n |
|---|---|---|---|
| 1 | Sleepy NAND | 1.713345e-007 | 1.202358e-007 |
| 2 | Noval Sleepy NAND | 4.317698e-009 | 4.195492e-009 |

*II. IN TABLE CMOS SLEEPY NOR AND NOVEL SLEEPY NOR GATE TOTAL (AVERAGE) POWER*

| S.no | Gate | Power(watt) at 65n | Power(watt) at 45n |
|---|---|---|---|
| **1** | Sleepy NOR | 1.648415e-008 | 5.850784e-009 |
| **2** | Noval Sleepy NOR | 4.317698e-009 | 3.93949e-009 |

## VI. CONCLUSIONS

An efficient method for reducing leakage current in VLSI design is presented in this paper. We have simulated the circuit design using 65 nm and 45nm CMOS NAND and NOR Gate technology files. We applied Sleepy Transistor technique and Noval sleepy to a chain of four inverter circuit. All the designs are developed in Tanner design environment with the total (average) power dissipation measurement. The novel sleepy transistor based design provides very good reduction of leakage power. The Noval sleepy transistor approach shows improved results in terms of power. It gives the CMOS circuit designers another option in designing integrated circuits more efficiently.

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