

Automatic Elevator Controller

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Abstract. The elevators have embellish as an important part of any commercial or public complex in this new era. because, of these elevators it becomes very easy and quick for people and luggage to move from one place to another place. Most of the control and industrial applications are running on the traditional PLC technology abundantly as PLC has flexibility, lower cost and security compared to other techniques, but still a powerful alternative for PLC is needed. In recent years, FPGA has been the best replacement of PLC to implement control algorithms in industrial, digital signal processing, video and audio applications as well to perform control tasks. The entire world is facing the pandemic situation and in this period there is a need of Automatic Elevators. Automatic elevators runs without having floor buttons pressed. When passenger enters and/or leaves the elevator cab, door sensors detects passengers as they enters and/or leaves. After the doors closed, the elevator will starts to run by it's own. Three level efficient elevator control system is designed by simply changing the state diagram, VHDL code is generated and used in Quartus to implement control system on FPGA Altera DE2-115. MODELSIM simulation software is used to simulate VHDL implementation of ourproposed Automatic Elevator.

1 Introduction

An elevator is used to transit the people or luggage between floors of a building or similar structure. This is the certification that allows people move with safety and convenience. The relay logic, PLC and microcontroller were used for the establishment of traditional elevator control system. The reduced number of inputs and outputs is the main disadvantage of this system. So, for the better solution for implementing an elevator controller one can use FPGAs [2].

Very Large Scale Integration is in demand all over the world due to the rapid development of the semiconductor industry over last 20 years. The design based on VLSI technology can be easily understood with the help of digital logic theory and techniques. To make the circuit fast and high speed these fundamentals are very important. As the technology is improving rapidly, the designs need to be made simpler for enjoying the benefits [3].

The concept of finite state machine technology is used for implementing on the elevator controller. The elevator process can be defined with the help of different states as per the FSM technology. In Elevator there will be a change from one floor to another floor which is based on the FSM technique that is the change from one state to another state

. The main aim is to design a minimum cost and compresscontroller prototype on VHDL. VHDL is a Hardware De- scription Language used in designing of digital circuits by describing digital models in a textual manner [1].

In this work, main approach was to develop an elevator algorithm for an elevator with multiple number of floors and by improving its efficiency. VHDL is a hardware de- scription language which is commonly used to describe digital circuits in a textual manner in designing. Project explains the design of elevator control system by using where VHDL code is generated using MODELSIM software. There is no need to write a complex code is the key point of our project, as needed in other control techniques. Automatic sanitization system is implemented with the ob- jective of minimum physical contact [3].

2 Literature Survey

In 312, Archimedes invented the first reference elevator. The elevator was developed with the help of cable on a rope and which was powered by hand. This kind of eleva- tor was established in the cloister of Egypt. In the building of England and France in 1792, the very small type ele- vators were placed. Lvan Kuliben in 1793, invented an elevator with the screw lifting mechanism in Saint Peters- burg. The safety elevator was invented by Elisha Otis in 1852, which restricted the fall of the elevator car, if the ca- ble broke suddenly. In New York City the elevator which was installed is used by the first Otis passenger in March 1857. In 1880 Werner Von Siemens invented the first elec- tric elevator. A method was patented by J.W. Meaker in 1874, which allowed elevator to maintain the safety while opening and closing of the door. A company named the Hydraulic Power Company was established in 1882 be- cause of the invention of hydraulic power technology [3]. The first residential elevator was created by the Clarence Conrad Crispin with inclinor company of america in 1929. In that first elevator there was a arrival sensor which gets detected when the elevator reaches on the respective floor. The another main element of the of elevator sys- tem is DC motor. DC motor works in either forward and reverse direction when the switch is being pressed. The computer is used nowadays to control many modern eleva- tors. The processing of the necessary information about the elevator is the computers job. To move the elevator carin correct position it is required to turn the motor correct amount. Right from the invention of the elevator nothing much has changed in the technology. [2].

This work based on the principle of minimum physical contact, which will be implemented with the help of Al- tera DE2-115 and the required sensors. In recent years, many different universities are working on this project [4].

3 Tools Required

3.1 Software

3.1.1 Quartus

Intel Quartus Prime is programmable logic device boards outlines software invented by Intel earlier to Intel's acqui- sition of Altera the tool was named Altera Quartus Prime, previously Altera Quartus II. Quartus Prime allow analysis and synthesis of HDL designs, which allows the developer to compile their designs, perform timing analysis, moni- tor RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the program- mer. An implementation of VHDL

and Verilog for hardware description, visual editing of logic circuits and vector waveform simulation is done with the help of QuartusPrime.

3.1.2 ModelSim

For simulating hardware description languages such as VHDL, Verilog and System C we use ModelSim which is a multi-language environment by Mentor Graphics. It includes a built-in C debugger circuit. Intel Quartus Prime, Xilinx ISE or Xilinx Vivado can be used with ModelSim, or ModelSim can be used independently with the system. The graphical user interface (GUI), or automatically using scripts is used to perform Simulation. For the MATLAB/Simulink, ModelSim can also be used. For such designs, MATLAB provides a numerical simulation toolset, while ModelSim provides tools to verify the hardware implementation timing characteristics of the design.

3.2 Hardware

Altera DE2-115 Board

The DE2 series has always been at the frontier of educational development boards. The newest DE2-115 that features the Cyclone IV E device by extending its leadership and success is announced by Terasic. Mobile video, voice, data access, and the desire for best quality images by responding to increased versatile low-cost it is needed to be driven by spectrum. The new DE2-115 comes with a perfect balance of minimum cost, minimum power and a rich supply of logic, memory and DSP capabilities.

The Cyclone EP4CE115 device features 114,480 logic elements which is the most offered in the Cyclone IV E series. It has 3.94 Mbits of RAM. It contains 266 multipliers. It gives us the best package of minimum cost and functionality, and minimum power in comparison with previous generation Cyclone devices.

4 Flowchart

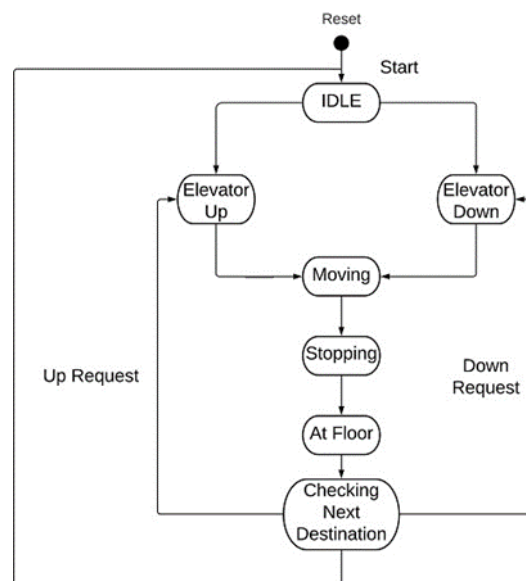


Figure 1: Elevator Controller Flowchart

- Initially the system is in the ideal state. the elevator will generally move in two state i.e up or down.
- If the elevator is moving in upward direction it will stop at desired floor and it will check for its next destination.
- And if the elevator is moving in downward direction it will stop at desired floor and it will check for its subse-quent destination.
- According to the request from any floor the elevator will either move in downward direction or upward direction.
- If the system is reset, it will arrive to its ideal position regardless of any request.

5 Algorithm

This algorithm is based on mathematical model of computation with the help of finite-state machine. The change from one state to another by giving output to some input is called transition. An FSM is defined with the help of different states, its inceptive state and the inputs that trigger every transition.

In modern world state machines can be observed in many devices as it performs predetermined series of action depending on sequence of events. Examples of which is vending machines used to waive products when the coins which are deposited are in proper combination. The second example of FSM is an elevator, according to the input given by person the elevator stop at desired floor. Another example is traffic light, when cars are waiting the pattern of signals get changed and Fourth example is of combination locks, which want the proper input to get the locked solved.

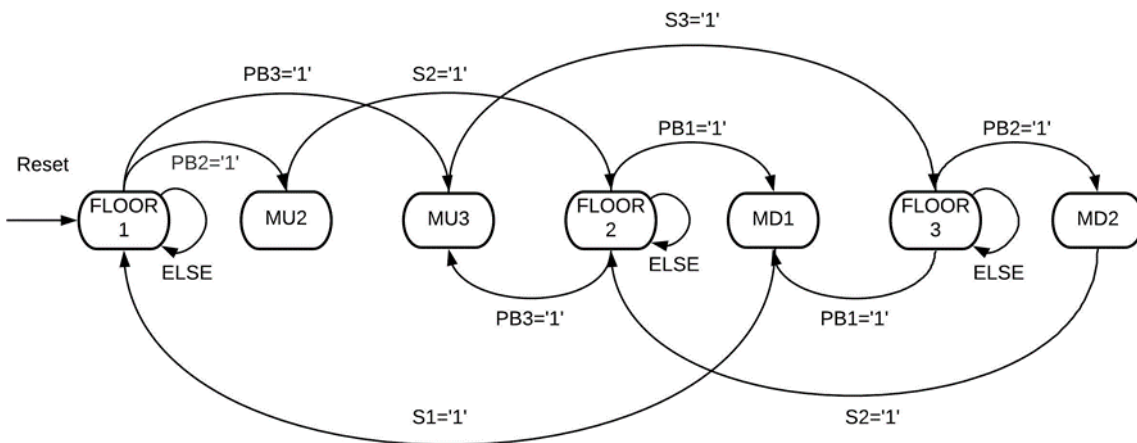


Figure 2: State Diagram

6 Result and Analysis

automatic elevator controller

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1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3
4 ENTITY elevator IS
5   PORT (
6     floor1: in std_logic;
7     floor2: in std_logic;
8     floor3: in std_logic;
9     reset: in std_logic;
10    );
11 ARCHITECTURE AutoElevator of elevator IS
12   TYPE state IS (F1, F2, F3, MU2, MU3, MD1, MD2);
13   SIGNAL pr_state, rn_state: state;
14 BEGIN
15   @PROCESS(reset)
16   BEGIN
17     IF (reset = '1') THEN
18       pr_state <= F1;
19       rn_state <= F1;
20     ELSE
21       pr_state <= pr_state;
22       rn_state <= rn_state;
23     END IF;
24   @PROCESS(pr_state, rn_state)
25   BEGIN
26     CASE pr_state IS
27       WHEN F1 =>
28         IF (floor1 = '1') THEN
29           rn_state <= F1;
30         ELSE
31           rn_state <= F1;
32         END IF;
33       WHEN F2 =>
34         IF (floor2 = '1') THEN
35           rn_state <= F2;
36         ELSE
37           rn_state <= F2;
38         END IF;
39       WHEN F3 =>
40         IF (floor3 = '1') THEN
41           rn_state <= F3;
42         ELSE
43           rn_state <= F3;
44         END IF;
45       WHEN MU2 =>
46         IF (floor1 = '1') THEN
47           rn_state <= F1;
48         ELSE
49           rn_state <= MU2;
50         END IF;
51       WHEN MU3 =>
52         IF (floor2 = '1') THEN
53           rn_state <= F2;
54         ELSE
55           rn_state <= MU3;
56         END IF;
57       WHEN MD1 =>
58         IF (floor1 = '1') THEN
59           rn_state <= F1;
60         ELSE
61           rn_state <= MD1;
62         END IF;
63       WHEN MD2 =>
64         IF (floor2 = '1') THEN
65           rn_state <= F2;
66         ELSE
67           rn_state <= MD2;
68         END IF;
69     END CASE;
70   END PROCESS;
71 END AutoElevator;

```

Figure 3: VHDL Implementation of this work

Referring to the VHDL implementation of this work, the state diagram is generated and with the help of Netlistviewer the RTL schematic is generated. Based on the work and by simulating this program the following results are received which are shown in below figures.

- Here, floor1, floor2, floor3 are indicating the three floors of the elevators.
- The two states MU2 and MU3 indicates that the motor is moving in upwards direction and at that time hbrg generate "01" output.

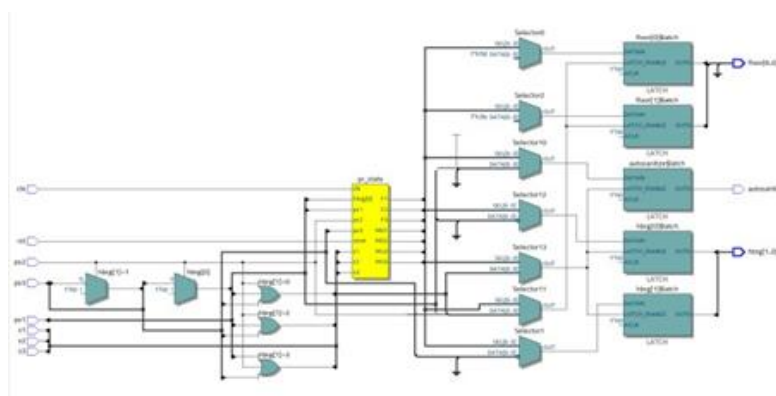


Figure 4: RTL Viewer

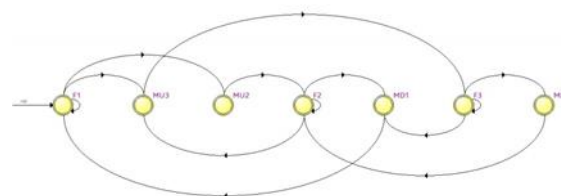


Figure 5: State Daigram

- Similarly, the other two states MD1 and MD2 indicates that the motor is moving downward direction and at thattime hbrg generate "10" output.

- PS1, PS2, PS3 are the inputs for floor1, floor2, floor3.
- S1, S2, S3 are the inputs for sensing MU2, MU3, MD1,MD2.

Referring to figure 6, Initially the elevator is on floor 1 when PS2 detects the person at that time the signal be- comes high and the state change from F1 to MU2 and hbrg becomes "01".That means the elevator is moving upwards. Now, the present state is MU2. so, when S2 equal to "1" the next state changes from MU2 to F2 and floor becomes"0000010" and hbrg results into "00" that means the elevator has reached to the desired position.

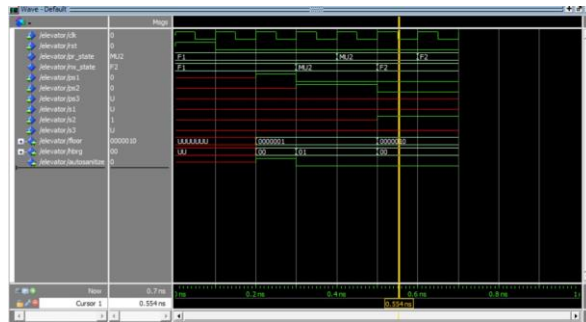


Figure 6: Transition from Floor1 to Floor 2

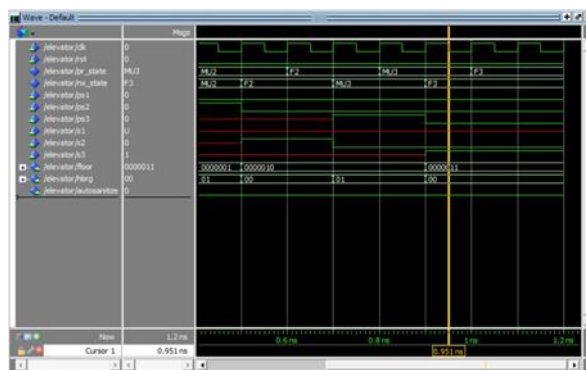


Figure 7: Transition from Floor 2 to Floor 3

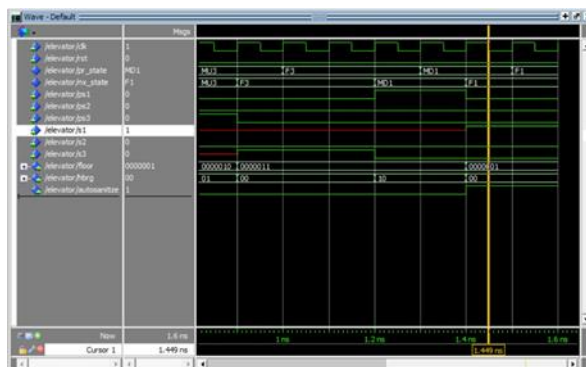


Figure 8: Transition from Floor 3 to Floor 1

Referring to figure 7, Initially the elevator is on floor 2 when PS3 detects the person at that time the signal be- comes high and the state change from F2 to MU3 and hbrg becomes "01".That means the elevator is moving upwards. Now, the present state is MU3. so, when S3 equal to "1" the next state changes from MU3 to F3 and floor becomes"0000011" and hbrg results into "00" that means the ele-

vator has reached to the desired position.

Referring to figure 8, Initially the elevator is on floor 3 when PS1 detects the person at that time the signal be- comes high and the state change from F3 to MD1 and hbrg becomes "10". That means the elevator is moving down- wards. Now, the present state is MD1. so, when S1 equal to "1" the next state changes from MD1 to F1 and floor becomes "0000001" and hbrg results into "00" that means the elevator has reached to the desired position. Here, the elevator has directly jumped from F3 to F1.

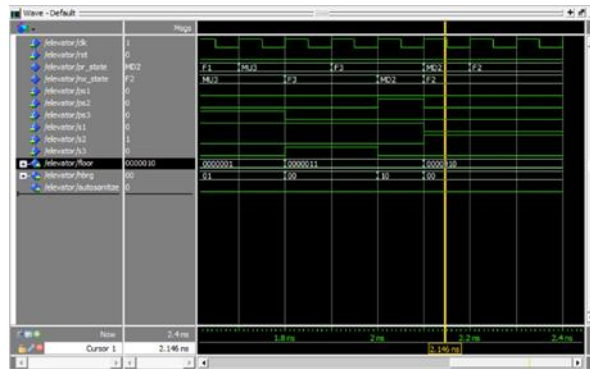


Figure 9: Transition from Floor 3 to Floor 2

Referring to figure 9, Initially the elevator is on floor 3 when PS2 detects the person at that time the signal be- comes high and the state change from F3 to MD2 and hbrg becomes "10". That means the elevator is moving down- wards. Now, the present state is MD2. so, when S2 equal to "1" the next state changes from MD2 to F2 and floor becomes "0000010" and hbrg results into "00" that means the elevator has reached to the desired position.

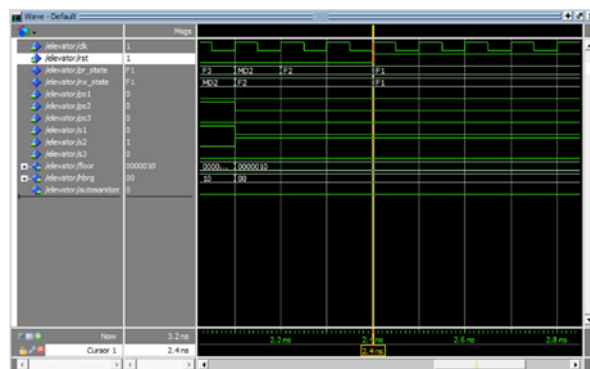


Figure 10: Reset Logic

Referring to figure 10, Initially the elevator is on floor2 as soon as rst=1 the elevator changes its state and come to its original position i.e floor 1. When rst=1 no operation will be perform everything will be at its initial position andwhen rst=0 all the functions will start their operation.

7 Conclusion and Future Scope

This work explains the finite state machine of the elevator control system which is implemented using Altera DE2-

115. Due to its wide range of pros compared to traditional schematic-based design the VHDL was

given key importance in designing. Here FSM is used to change the state. Flowchart, algorithm and state diagram is designed for implementation of this project. Auto sanitization system is also implemented in this elevator, as the main objective of the project is to focus on the principle of minimum physical contact.

VHDL implementation of this code will be implemented on the hardware and will meet necessary modification whenever some new aspects will be encountered which should be improved. The number of sensors will increase as we make progress on this project. There is a scope that once the person leaves the car, the fans and lights will turn off automatically. IoT based digital voice assistant services like alexa, siri can also be implemented in the elevator.

References

- [1] H.P.A.P. Jayawardana, H.W.K.M. Amarasekara, P.T.S. Peelikumbura, W.A.K.C. Jayathilaka, S.G. Abeyaratne, S.D. Dewasurendra, "Design and implementation of a statechart based reconfigurable elevator controller" International Conference on Industrial and Information Systems - ICIIS, 2011 IEEE
- [2] S. Ichikawa, M. Akinaka, R. Ikeda, H. Yamamoto, "Converting PLC Instruction Sequence into Logic Circuit: a Preliminary Study," IEEE International Symposium on Industrial Electronics, pp. 2930-2935, 2006.
- [3] J. J. Rodriguez-Andina, M. J. Moure and M. D. Valdes, "Features, Design Tools and Application Domains of FPGAs," IEEE Trans. On Industrial Electronics, vol. 54, no. 4, pp. 1810-1823, Aug. 2007.
- [4] Sithumini Ekanayake, Ruwan Ekanayake, Somasundaram Sanjayan, Sunil G. Abeyratne, S.D. Dewasurendra "FPGA Based Elevator Controller with Improved Reliability" ,2013 UKSim 15th International Conference on Computer Modelling and Simulation IEEE.
- [5] Monzurul Islam Dewan, Md. Arafat Mahmud, Md. Tashfiq Bin Kashem, Mushfika Baishakhi Upama, "A Simulation Study of Elevator Control of a Building using Digital Logic Circuit", IOSR Journal of Engineering Vol. 3, Issue 12 (December. 2013)
- [6] P. Rajesh, "Design and Implementation of Embedded Based elevator Control System," M Tech thesis, 2010.
- [7] A VLSI Implementation of Three-Lift Controller Based on Verilog by Patchala Kiran Babu, H. Raghunath. International Journal of Engineering Trends and Technology (IJETT), Volume 6 Number 1-Dec 2013.
- [8] M. S. Siddiqui, and K. Hasan, "Synthesis and simulation model of parallel lift controller using verilog," International Journal of Engineering Development and Research vol. 3, pp. 1-3, 2015.
- [9] P. K. Babu, and H. R. Rao, "A VLSI implementation of three-lift controller based on verilog, International Journal of Engineering Trends and Technology, vol.6, pp. 43-48, 2013.
- [10] Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, Michael Wirthlin, "Improving FPGA Design Robustness with partial TMR", Reliability Physics Symposium Proceedings, 2006 IEEE.
- [11] Karl Schabas, Stephen D. Brown, "Using Logic Duplication to Improve Performance in FPGAs", University of Toronto, Toronto, Canada
- [12] S. K. Wood, D. H. Akehurst, O. Uzenkov, W. G. J. Howells, and K. D. A. McDonald Maier, "A Model-Driven Development Approach to Mapping UML State Diagrams to Synthesizable VHDL," IEEE Transaction on Computers, vol. 57, 10, pp. 1357-1371, 2008.
- [13] J. Becker, G. Hettich, R. Constapel, J. Eisemann, J. Luka, "Dynamic and Partial FPGA Exploitation," in Proceedings of IEEE, vol. 95, no. 2, February 2007.
- [14] P Bala Gopal, K Hari Kishore, B. Praveen Kittu "An FPGA Implementation of On Chip UART Testing with BIST Techniques", International Journal of Applied Engineering Research, ISSN 0973-4562, Volume 10, Number 14, pp. 34047-34051, August 2015.
- [15] A Murali, K Hari Kishore, D Venkat Reddy "Integrating FPGAs with Trigger Circuitry Core System Insertions for Observability in Debugging Process" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.11, Issue No.12, page: 2643-2650, December 2016
- [16] Cristiana Bolchini, Antonio Miele, Marco D. Santambrogio, "TMR and Partial Dynamic Reconfiguration to mitigate SEU faults in FPGAs", International Symposium on Defect and Fault-Tolerance in VLSI Systems-DFT '07, 2007 IEEE
- [17] Michael D. Ciletti, "Advanced digital design with the VERILOG HDL", Prentice-hall of India ltd, India

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- [18] <https://www.intel.com/content/dam/altera-www/global/enUS/portal/dsn/42/doc-us-dsnbk-42-1404062209-de2-115-user-manual.pdf>
- [19] Volnei A. Pedroni, Circuit Design and Simulation with VHDL", MIT Press