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Design and Analysis of Low Power High Speed Sense Amplifier for Memory Application

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Abstract: Sense amplifiers are extensively used in memory. Sense amplifiers are one of themost vital circuits in the periphery of CMOS memories. We know that memory is the heart ofall digital systems. Today all worlds are demanding high speed and low power dissipation aswell as small area. We know that speed and power dissipation of memory is overall dependsupon thesenseamplifierweused and theirperformancestronglyaffects both memoryaccess time, and overall memory power dissipation. So it is important to design a goodsense amplifier which performs well in both speed and power dissipation. In this dissertation,an implementation of a most efficient sense amplifier is done by comparing the best knownsense amplifier in today.The dissertation focuses on design, simulation and performanceanalysis ofsenseamplifiers.

In this paper, current latch sense amplifier and body bias controlled current latch senseamplifier are designed and results compared. The result shows that the body bias controlledcurrentlatchsenseamplifierisperformingbest.Theresultalsoshowsanovelsenseamplifier which consumes small power at same time its speed is faster than other senseamplifiers.

Allthedesignshavebeenimplemented,synthesisandsimulatedon180nmCMOStechnology usingtanner tool version16.1.

Index Terms— Sense amplifier, offset in sense amplifier, advanced current latched sense amplifier, recharged circuit.

INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digitalsystem has adequate memories. In memory today the CMOS memories are used in a

muchgreater quantity than all the other types of semiconductor integrated circuit. SRAMs areused as large caches in microprocessor cores and serve as storage in various inputs on asystem-on-chip like graphics, audio, video and image processors. SRAMs also used in highperformancemicroprocessorsandgraphicschipssoforeachgenerationtobridgetheincreasing divergence in the speeds of the processor and the main memory we need highspeed requirements.At the same time, SRAMs used in application processors which go intomobile,handheldandconsumerdeviceshave verylowpowerrequirements.Sopowerdissipation has become an important consideration both due to the increased integrationandoperatingspeeds,aswellasduetotheexplosivegrowthofbatteryoperatedappliances. Aswithotherintegratedcircuitstoday,CMOSmemoriesarerequiredtoincrease speed,improvecapacityandmaintain lowpower dissipation.

To read the contents of this memory a sense amplifier is used. The sense amplifier convertsthe arbitrary logic levels of bitlines to the digital logic levels which required running theperipheral Boolean circuits of outside world of memory. In the SRAM data path, switching ofthe bitlines, I/O lines and biasing the sense amplifiers consume a significant fraction of thetotal power. Mainly performance of memory depends on the performance of SA such asdelayandpowerdissipation.

So the sense amplifier is one of the most circuits in the periphery of CMOS memories. Speedand power dissipation of the memory is mainly depends on types of sense amplifier used. Soperformance of SA strongly affects both memory access time, and overall memory powerdissipation.

Power dissipation was not the main issue' just proper output and the circuit operation wasthemainpreference.Thelowpowerintendincircuitdesignisused becauseof:

1. Ifthesystemdissipateshighpower,thenextradesignisrequiredforthecoolingsystem,thusth esystemwillbecomeverybulkyandwillnotbeportable
2. Duetotheextracoolingsystemthecostofthesystemwillincrease.
3. Due tothesky-scraping power dissipation theperformance and reliability of thesystemdecreases
4. Memory is the main and important field of design.Today the size of the memory isdecreasing and the storing capacity is increasing.Asthestoringcapabilityisincreasing,thetimeresponseforthedatawritingandreadingfro mthememory should be very fast. For this purpose different types of sense amplifiers areused.

NECESSITYOFSENSEAMPLIFIER

Inthememory,itiscommontoreducethevoltageswingonthebitlinestoavaluesignificantlybelowthe supplyvoltage.This reduces both the propagation delay and thepower consumption.Noiseand otherdisturbances may be occurredinthe memoryarrayfor this sufficientnoise marginis obtainedevenfor these small signalswings. During theinterfacing of the memory to the external field, the amplification of the internal swing isrequired.This is achieved by the sense amplifiers.Designofahighperformanceandefficientsenseamplifierisveryimportantfordesign SRAMSbutwithincreasingparameter variations, the developing of a reliable and fast senseamplifier isa big problemin itself Senseamplifiersplayamajorroleinthefunctionality,performanceandreliabilityof memorycircuit.Reductionindelayandpowerisacquiredbyusingsenseamplifierinmemorycircuits. The designed sense amplifier should be standard and capable to support the current SRAMdesignwithoutsignificantlyaffectingtheotherdevicesofperipheralsofSRAM.

BASICOFSENSEAMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation froman accessed memory cell to the logic circuit located at the periphery of the memory cellarray, and used to detect small variation on bitlines of memory and produce full voltageswing it means that converts the arbitrary logic levels occurring on a bitline to the digitallogic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operatewithin the conditions which are set by the operation margins. Operation margins in a digitalcircuit are those domains of voltages, current and charges. These domains unambiguouslyrepresentdatathroughouttheentireoperationrangeofthecircuit.Operationmargind epends on the circuit design, processing technology and environmental conditions. Senseamplifiers, usedwithmemorycells,arekeyelementsindefiningthe performanceandenvironmentaltoleranceofCMOSmemories.Becauseoftheirgreatimportancein memory designs, sense amplifiers became a very large circuit-class. CMOS memories are used in amuch greater quantity than all the other types of semiconductor integrated circuits, andappearinanamazing variety of circuitorganizations.

Memory Sensing and amplifying the information signal which transfers over memory cell tobit lines are the most important ability for a sense amplifier. However, to sense the datacorrect and fast turn into more and more difficult when the operational voltage scales downto low voltage. In an integrated circuit "sensing" means the recognition and resolve of thedata content of a selected memory cell. The sensing may be "nondestructive," when theinformationcontentoftheselectedmemorycellisunaffected(e.g.,inSRAMs,ROMs,PROMS, etc.), and "destructive," when the information content of the selected memory cellmaybealtered(e.g.,inDRAMS,etc.)bythesenseoperation.Sensingisperformedinasensecircuit.

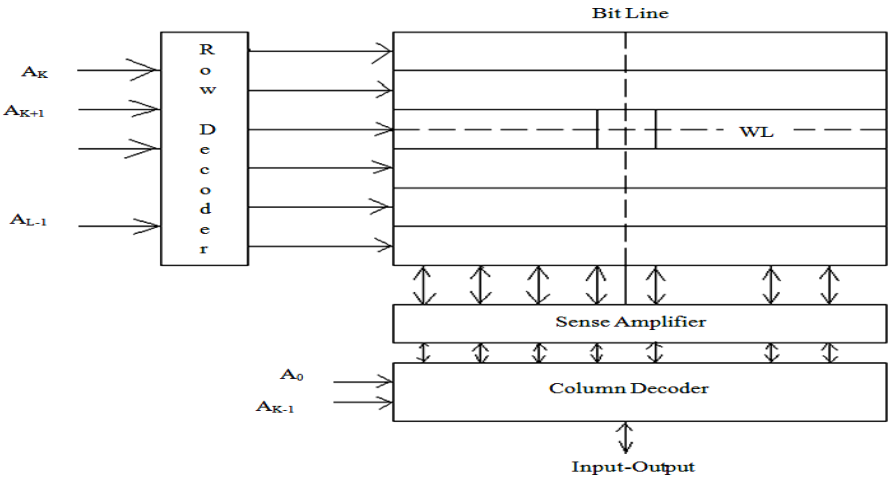


Fig.1MemoryArchitecture

DESIGNIMPLEMENTATIONANDSIMULATIONOFSENSEAMPLIFIERS

On the moderntrends quick memories are highly requiredwithlow powerconsumption.The low power and low voltage CMOS techniques were applied extensively in analog andmixed mode circuits for the compatibility with the present IC technologies. Low powerconsumptioncanbeachievedbyusingsenseamplifierswhicharemainpartof CMOSmemory. Parasiticcapacitanceismuchhigherifmemoryisofhighdensity.Thelargecapacitance is an issue to make our each cell more energy to charge means low to senseamplifier. To achieve a faster memory and less power dissipation we have to design senseamplifiersas.Increaseinnumberofcellsperbitlinewhichwillincreasetheparasiticcapacitance. Minimizesupplyvoltageleadtoshortnoisemarginthataffectsthesense amplifier reliability. To maintain small voltage swing over the bit line, increase the area ofeachcellfordesignmorememoryonthechipwhichdecreasedtheloadonbitline.Thewide range of

applications of sense amplifier as it provides a photovoltaic system whichusually stores enough energy for uncertainty in availability of solar radiation due staticallynature of biosphere. These typical ICs are the complex component to measure the chargebattery and discharge current. sense amplifiers plays a very smart role to maintain thereliability , accuracy and extended battery life by cutting power down over certain region tocontrol heat. Mainly two types of SRAM sense amplifier linear amplifier and latch typeamplifier.

As previously discussed in chapters about various sense amplifiers, it is found that somesense amplifier consume less power but with more delay than other consume slightly morepower but speed (with less delay) is relatively large. In this dissertation I propose a newsensing scheme which has less delay, more sensitivity than previously discussed with lesspowerconsumption.Thischapterdividedintofourparts.

- Currentlatchsenseamplifier
- Latchoperation
- TheSizingConsideration
- Body-biasedcontrolledCurrentlatchsenseamplifier

ThesesenseamplifiersmadeusingwiththehelpofTannertoolV13.1.

CURRENTLATCHSENSEAMPLIFIER(CLSA)

Latch-typesenseamplifiers,orsenseamplifierbasedflip-flops,areveryeffectivecomparators.Theyachievefastdecisionsduetoastrongpositivefeedbackand theirdifferential input enables a low offset. The sense amplifiers circuit is the heart of memory.The sense amplifiers are mainly designed to read the memory contents and amplify them toproper level using at logic circuits around memory. Sense amplifiers (SA) are hence widelyapplied in, for example, memories, A/D converters, data receivers and lately also in on-chiptransceivers have become especially popular because of their high input impedance, full-swingoutputandabsenceofstaticpowerconsumption.AgoodSAhasthefollowingproperties namely, minimum sense delay, minimum power consumption, proper gain foramplification, minimum layout area, highly reliable, less number of cascading of transistorsfromsourcevoltage togroundforlowvoltageoperationandtolerable toenvironment.Thiskindofsenseamplifiercircuitisdesignedforincreasedspeed,sensitivitywithreducedpowerconsumption.Thisdesigncombinesaspectsfromthelatchbasedvoltagemodesenseamplifierandthedifferential CurrentLatchSenseAmplifierisbasedonvoltagemodesenseamplifier.Itisalsoclassifiedindifferential type voltage sense amplifier. In this amplifier two cross-coupled inverters areused which give positive feedback as in latch type sense amplifier. But here the

bitline isisolated from its output by using extra two nMOS transistors. Soit has very high inputimpedance.TheCLSAisshowninFig2

CIRCUITCONFIGURATION

Itconsistsof5nMOSand4pMOStransistorsnamelyMN1,MN2,MN3,MN4,andMN5.

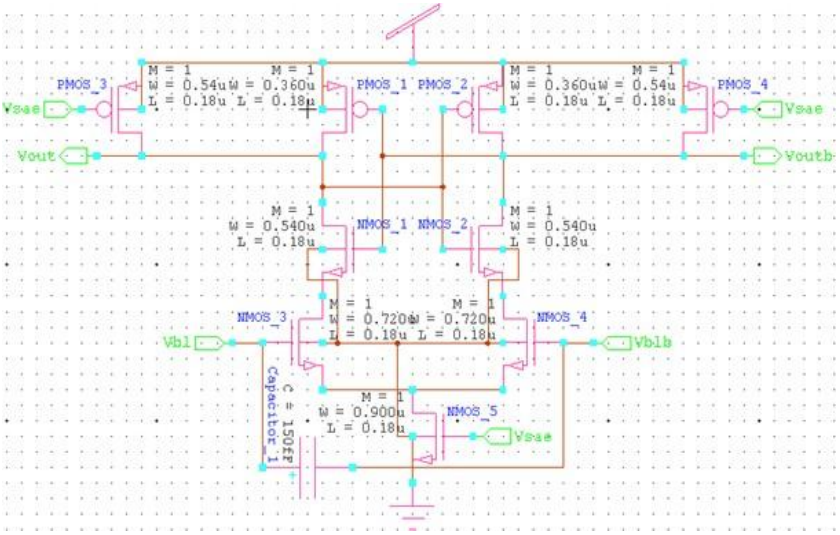


Fig.2CurrentLatchSenseAmplifier(CLSA)

MN1, MP1, MN2 and MP2 make two inverters connected in cross coupled manner givepositive feedback in circuit.MN3 and MN4 are used to couple bitlines to CLSA amplifier.MP3and MP4 are precharge transistors. The capacitor C represents the column capacitance ofbitlines for filling of SRAM in circuit. The sense amplifier has following ports namely Vsae,vout, voutb, bl, blb. The bl and blb are column bit lines of SRAM. The signals are given to the**Vsae**which control the precharge and enable CLSA.The amplified output is taken from **Vout**nodeandcomplimentaryoutputat**Voutb**node.

WORKINGOFCURRENTLATCHSENSEAMPLIFIER(CLSA)

The sense amplifier is pre-charged in other words it is reset before sensing the bitlines. Thisactionclearsthepreviouslylatcheddataandchargedtheoutputnodestothesupplyvoltage.

Whenthecontrolsignal**Vsae**,isat0logicmeans(lowvoltage)thepre-chargetransistorMP3and MP4 turned on so the output nodes are charged to supply voltage V_{DD}. When the senseamplifier enable signal Vsae is at high, the precharged transistors MP3 and MP4 turned off.But at this time transistors MN5 turned on so the drain of MN5 is pulled down to groundlevel.Duetothisnow,transistorsMN3andMN4areworkingasacommonsourcedifferentialamplifier.

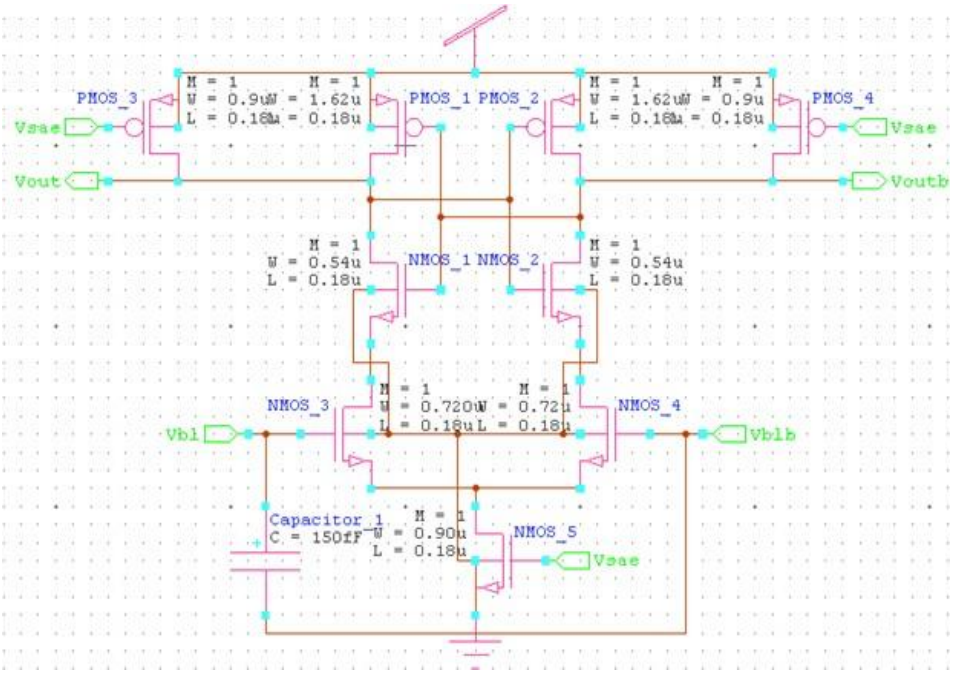


Fig.3CurrentLatchSenseAmplifier(CLSA)withdifferentW/Lratio

Due to the voltage difference developed by bit lines, bl and blb is transferred to drain nodesoftransistorsbythecommonsourcedifferentialamplifier.AtthistimeVoutandVoutbstartsdischargingsupposeblatV_{DD}andblbatV_{DD}-ΔVvolts.Thisresultgivesmorecurrentflowthru MN3 than MN4.Due to this **Vout**node discharged rapidly than **Voutb**. Because out noderapidly discharging, when it reach at enough low level of voltage at this time the MN2 startstoonstate.Sotheveryhighpositivefeedbacksloopworkveryinventively.Thisactioncausesout b node charged to V_{DD} level and out node to ground GND. Here transistor MN5 works ascurrent source and transistor MN1, MP1, MN2 andMP2 work as latch and produce very highgain due to positive feedback. The speed of sense amplifier is depends on the how fastoutput nodes get charged thru pre-charging transistors. So by proper design pre-charge timekept as small as possible. CLSA performed sensing and amplification using withoutanycurrentfrombitlinestooutputssothesenseandpre-chargepowerdissipationcanbe reduced.Themaindrawbackisthatituse4stagesoftransistorcascadedfromV_{DD}toGND.Itgive results that CLSA not work at very low voltage due to very low differential current sospeedisslowatlow$V_{DD.}$

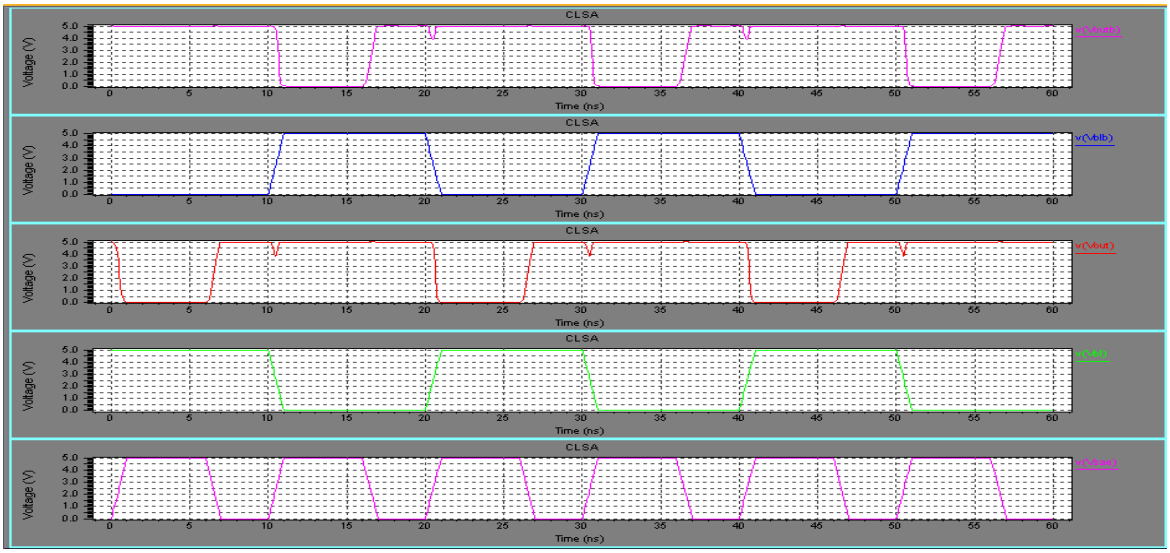
RESULTANALYSISANDCOMPARISON

InthischapterhereweshowthattheSimulationresultsofallimplementedsenseamplifiers.Function of designs is verified by using simulated based verification. This verification ensuresthat the design is functionally correct when tested with given set of inputs. Designed

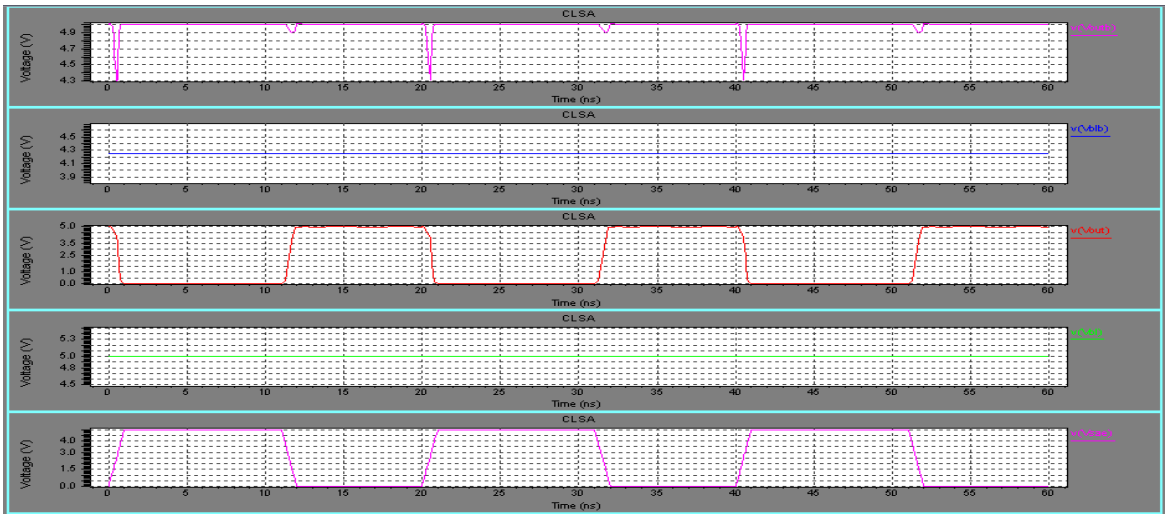
senseamplifiershavebeenimplementedandsimulatedonTannertoolin180nmtechnology.

CurrentLatchSenseAmplifier(CLSA)

In this section I show the simulation results of Current Latch Sense Amplifier (CLSA). Thesimulation time is taken for CLSA amplifier is 60 neno seconds. The simulation waveform ofthe CLSA is shown in figure 5.1.Figure 5.1(a) shows the simulation waveform of the CLSA atV_{DD}=5Volt. V_{sae} given in pulses of 0.5 duty cycle with time period of 10n seconds both rise andfall time is 1n seconds. Similarly bit input to V_{bl} is in bit form and in sequence of 10101 andinverseofthisis$V_{blb.}$Thetotalsimulationtimeis60nseconds.



(a)



(b)

Fig.4SimulationwaveformsoftheCurrentLatchSenseAmplifier(CLSA)(a)forBitVoltage(b)

ForConstantVoltageDifference

Similarlyfigure5.1(b)showsthewaveformatVDDat5volts,Vblat5voltsandVblbtakenat 4.25volts.Thefunctionallythisisshowninwaveformthatwhen Vsaeisatlowvoltsseeninv(Vase),the amplifierpre-chargedtoVDD.WhenVsaeisathighlevelthensenseamplifierisinsensing mode so Vout should be 0volt if Vbl is at 5volt otherwise if Vblb is at 5 volts its valueatfullswingvaluewhichis5volts.WeobtainedreversevalueforVoutbnodewhichisshownasV outbvalue.

Table1CLSAoperation

Vsae	Vbl	Vblb	Vout	Voutb	Remark
5V	5V	4.5V	0V	5V	Insensemode
0V	5V	4.5V	5V	5V	Inpre-chargemode
5V	4.5V	5V	5V	0V	Insensemode
0V	4.5V	5V	5V	5V	Inpre-chargemode

Thisisalsotrueforpulseinputs.

PowerdissipationofCLSA

Thefigure4showsthepowerdissipatedbytheCurrentLatchSenseAmplifieratVDDequalto3V.This dissipationismeasuredfor100nseconds.

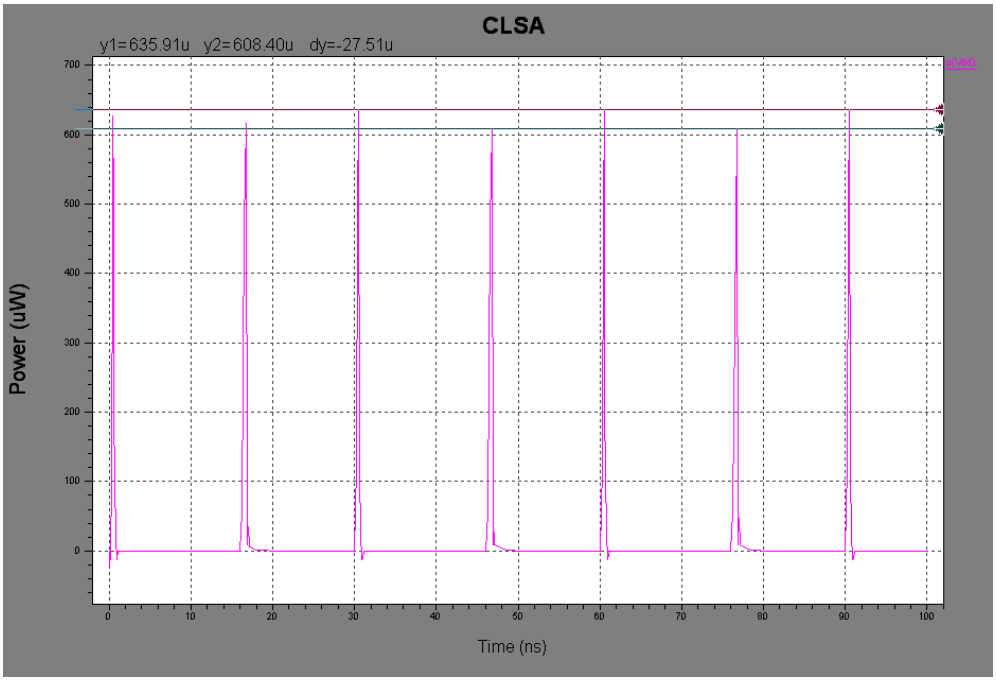


Fig.SimulationwaveformofpowerdissipationofCLSA

Table2 V_{DD} versus Pre-Charge Delay, Power Dissipation and Noise Margin of BB-CLSA

V_{DD} (V)	Pre-Charge Delay (ps)	Power Dissipation(µW)	Noise Margin V_{IL} (V)	Noise Margin V_{IH} (V)
5V	179	120.505	1.825	2.64
4V	211.13	74.045	1.315	2.06
3V	221.98	28.13	0.680	1.51
2V	241.04	12.695	0.605	1.055
1V	467.59	5.25	0.436	0.628

CONCLUSION AND FUTURE SCOPE

Conclusion

In this dissertation Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of tanner tool at a various supply voltage from 1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.
- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
- Noise Margin and Sensitivity of proposed sense amplifier is improved considerably.
- Body Bias method is used for high speed at low power dissipation operation.
- Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

Future Scope

However some aspects of the goal have been achieved using this design, but still a better Sense Amplifier can be build by some improvement in the circuit design. The SA can be further extended and modified by the following points.

- Delay can be further reduced by improving circuit design.
- Affect of process variations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations.

- Yieldmeasurementscanbedone
- The layout can also be designed using L-Edit of tanner tool by which area can becalculatedforchipfabrication.
- BodyBiasVoltageLatchSenseamplifierisdesignedforhighspeedoperation.
- In this design we use 180 nm technologies but latest technology 28nm and more canbeusedforbatterdesignandanalysis.
- The layout can also be designed using L-Edit of tanner tool by which area can becalculatedforchipfabrication
- Thedelayandpowerdissipationcanalsoreducedbyusinglowpowerandhighspeed techniques like VTCMOS, DTCMOS, and Adaptive CMOS and Adiabatic logictechnology.

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