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Single-Phase Switched-Capacitor Integrated-with Five-level boost Inverter

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Abstract- Multilevel inverter configurations are a great choice for medium and high power applications. This paper describes a novel five-level (2Vdc, Vdc, 0, Vdc, 2Vdc) boost multilevel inverter based on a single capacitor. The suggested single-phase arrangement has a single dc supply, eight switches, and one capacitor. The capacitor is charged in parallel and discharged in series connections while the inverter is operating in the charge-pump mode, which produces a greater output voltage. The suggested design calls for straightforward control operations, and a level-shift pulse width modulation technique is employed to drive the switches and provide the necessary pulse pattern. With this technique, the reference signal is compared to four carriers. The created inverter has a number of unique qualities, including its small size, simple control needs, boosting capabilities, and use of just one capacitor and one dc source. To assess the effectiveness of the created five-level architecture, the system is simulated using MATLAB/Simulink. The outcomes demonstrate that the constructed five-level multilevel inverter operates as predicted.

Index terms: Capacitor, Multilevel inverter Phase shift PWM, Simulink/Matlab

I. INTRODUCTION

Renewable In order to produce an output of alternating current with a particular amplitude, frequency, and harmonic character, dc to ac conversion is often needed. Pulse width modulation (PWM) inverters with two or more levels are the most popular ac/dc power electrical interfaces. They enable the amplitude, frequency, the output voltage's harmonics, as well as both. Lower harmonic components can be found in multilevel inverter designs' ac output. Multilevel inverter topologies have been extensively discussed in the literature [1–9] due to their advantages, such as small increased output waveform and filter size. A multilayer inverter makes use of several dc levels to produce a staircase waveform utilising power semiconductors. In terms of the harmonic profile and semiconductor voltage stresses, multilevel inverters perform better than two-level traditional inverters. [10].

A multilayer inverter's power quality gets better as the number of levels rises. On the other hand, raising the levels causes the development of numerous power semiconductors and the associated driving circuits. High system costs and complexity result from this. System efficacy and dependability are affected [10, 11]. Several multilayer inverter configurations were created. Among the configurations are cascaded H-bridge and neutral point clamped (NPC) (CHB), Modular multilevel converters and flying capacitors (FC) [12–15]. These or n-level output voltages can be produced using multilevel approaches [16]. Akira Nabae and Akagi(17) invented the NPC inverter

as a three-position diode clamped interpretation for motor drive. Despite just having one dc source, this architecture is focused on preserving the stability and equilibrium of the dc capacitors. The capacitor voltage and current are adjusted to preserve the stability and balance of the two heaps while the dc- capacitance is supplied by the dc- source [18]. Stillwell and Pilawa-Podgurski [19] used an FC multilevel converter to clamp the voltage of one capacitor voltage-level in place of a clamping diode. Due to its phase redundancy, the FC multilevel inverter varies from its NPC relative. The FC may be flexible and tolerate voltage unbalance or errors during charging or discharging thanks to this attribute. Moreover, redundancy heightens voltage stresses and harmonic profiles across power switches. However, the FC multilayer inverter has a number of drawbacks, such as ineffective switching efficiency and complicated control to regulate the voltage of all capacitors [15, 18]. The CHB multilevel converter, which comprises of series-connected h-bridge inverters, is another type of multilevel inverter.

Each bridge has its own independent dc power source. This arrangement has a distinct feel due to its modularity. In compared to neutral point and FC outcomes, it provides the inverter with superior fault forbearance and low power operation following cell loss [20]. A more distant source of electricity is multilevel, scalable, or modular technology inverters setting up multilayer inverters when any number of layers are required and separate control system-equipped sub modules are linked together in a cascade configuration. Due to the fact that current flow controlling modular multilevel topologies is a first-time challenge since it increases total system conduction losses within the motor. In this paper, a novel five-position boost inverter is described. In the literature, a number of five-position layouts are presented. Six switches, two diodes, and two capacitors can be used to change the five-position construction shown in Figure 21 into a five-position arrangement. Despite the smaller switches, the system's efficacy suffers because balancing the capacitors and diodes requires a sophisticated control algorithm. Similar to the arrangement in [21], the system in [22], which is based on a switched capacitors cell, aims to produce nine scenarios rather than five situations. Inverter with switches across it grounded on capacitor transformers with switches was developed by Roy et al. [23].Even though the five-level form uses the ideal number of switches and two capacitors, the control's complexity increases. Another recognisable There is a five-position structure in (24). Still, to create the required five-position affair, seven switches, four diodes, and two capacitors are needed.

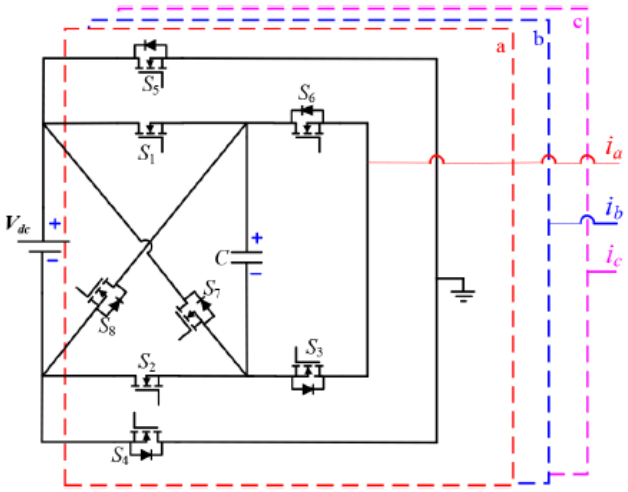


Fig. 1 The main schematic for the suggested five-position inverter is shown.

The various inverter designs suggested in have been updated for the recently proposed structure [25, 26]. Nonetheless, they contain two dc sources with distinct voltage boundaries and six dc sources grouped in three phases. The topologies shown in [25, 26] can yield nine circumstances. The proposed interpretation in this study can work in three phases with just one dc source and one capacitor while supplying a five-position affair voltage with just one dc source. Due to its boosting characteristics, this interpretation has an advantage over its equivalent in [25, 26] where the input voltage is greater than twice the affair voltage.

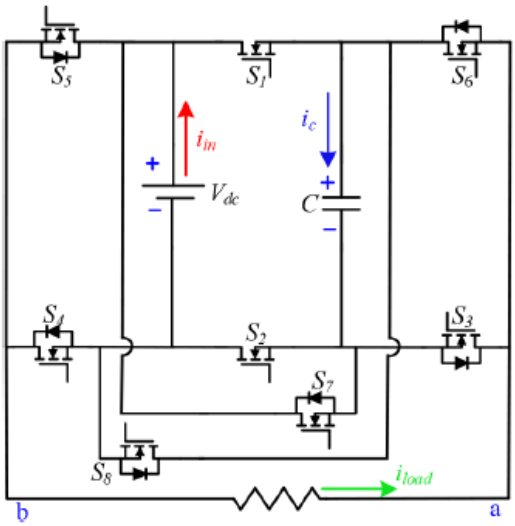


Fig. 2 shows the single-phase configuration of the five-position inverter.

The suggested arrangement produces a Using just one dc source, one capacitor, and eight power switches, it is feasible to generate a five-position affair voltage with a breadth twice as large as the input voltage. The circumstances of the generated affair voltage are as follows: (2Vdc, Vdc, 0, Vdc, 2Vdc). Figure 1 displays an academic design of the proposed system. Three capacitors and 24 power switches must be added in order to convert the system to three-phase operation. In this study, only single-phase designs will be investigated and assessed. The capacitor and the dc source being charged may occasionally be connected similarly. In order to provide an output voltage level of 2Vdc, a second series connection is made to the dc source. Position-shift PWM is used in this work to operate the multilayer inverter's switches (LS- PWM). To determine the required switching countries, four carriers are contrasted with the reference voltage. The investigation is structured as follows. The functioning of the designed multilayer boost-inverter is covered in section 2 section 3 of this article discusses the modulation approach, Section 4 discusses the suggested configuration's loss computation, and Section 5 discusses the simulation findings.

II. PROPOSED SECTION OF A FIVE-LEVEL BOOST MULTILEVEL INVERTER

The suggested five-position boost multilevel inverter is shown in Figure 2. A five-position multilevel inverter with boosting capacity and an affair voltage twice as high as the input voltage make up the suggested configuration. Only eight switches make up the defined topology, and two of them lack anti-parallel diodes. Table demonstrates that just six switching nations are actually required to produce the five-position affair voltage, even though there are 28 switching countries that might be used in the suggested inverter figures 3 and 4 show illustrations of each of the permissible operation modes.

A. Operation modes

Mode 1: Capacitor C charges from the dc source when the inverter occurs and the output voltage is zero (see Fig. 3a). Although the other switches were off, the switches S1, S2, S3, and S5 were activated, and the capacitor was employed in the analysis. The voltage of capacitor C is equal to the voltage of the dc source from which it draws its charge. Despite the fact that the positive affair terminal b is linked to the positive outstation of the input source, the negative outstation of the dc source is connected to terminal a.

Mode 2 when switches S3, S5, and S8 are on and the other switches are off; the inverter generates an affair voltage that is twice as high as the input voltage (see Fig. 3c). The output positive outstation is connected to the dc source's positive outstation, and terminal an is connected to capacitor C's negative outstation and when the other switches are off, switches S1, S2, S3, and S5 are turned on. Capacitor C has the same voltage as the dc source from which it receives its charge. Although the negative outstation of the dc source is connected to terminal a, the positive outstation of the input source is connected to terminal b.

Mode 3: When switches S3, S5, and S8 are on and the other switches are off, the inverter generates an affair voltage that is twice as high as the input voltage (see Fig. 3c). The affair's positive outstation is wired to the positive terminal of the dc source and terminal and is wired to the negative terminal of capacitor C.

Mode 4, Capacitor C is charged from the dc supply with a zero affair voltage. (See Fig. 4a in Fig. All the switches are inoperative besides S1, S2, S3, and S4. C, which has the same voltage as the dc source, is charged by the dc source. The input voltage charges C, and its steady-state value equals the input voltage. Both output terminals b and a are connected.

Mode 5: All switches are on, with the exception of S1, S2, S4, and S6. In this mode, the inverter generates an output voltage that is equal to the input voltage (see Fig. 4b). C receives its charge from the same DC source and has the same voltage as the DC source. When output positive terminal b is connected to the outstation of the dc-negative source, outstation an is linked to the outstation of the dc-positive source.

Mode 6: When S4, S6, and S7 are turned on while the other switches are off, the inverter creates twice the input voltage as affair voltage (see Fig. 4c). The capacitor C's positive outstation is linked to terminal and, which also serves as the dc-negative source's outstation. The outstation of the dc-negative source is connected to the output positive terminal b, and the positive terminal of capacitor C is connected to its positive outstation.

B. Deciding upon parameters

A low capacitor voltage ripple is essential because a high capacitor voltage ripple could generate an imbalance in the output voltage steps. In accordance with the analysis shown in numbers 3a, b, and 4a, C is charged by the dc source and matched with it. The impact of the following point equations

$$V_c = V_{dc} \leftrightarrow i_c = i_{in} \quad (1)$$

C is still charging in the manner depicted in Fig. 4a. Nonetheless, its present equation is distinct from the one given above and might be referred to as

$$V_c = V_{dc} \leftrightarrow i_c = i_{in} - i_{load} \quad (2)$$

The capacitor characteristics equation is applied when C discharges in the modes shown in Figs. 3c and 4b.

$$V_c = V_o - V_{dc} \leftrightarrow i_c = i_{in} \qquad (3)$$

Figure 5 displays a capacitor voltage curve. Following selection of C from the graph and choices (1-3) might be made:

Table-I

Demonstrates the five states of an inverter's switching

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

$$C = \left(\frac{V_o - V_{dc}}{2\Delta_{V_c}}\right) DT_s \quad (4)$$

C is influenced by the vdc input voltage, vo output voltage, Ts sampling period the allowable capacitor voltage ripple vc, and the duty ratio D. Table 2 provides a summary of the voltage and current pressures on various components. Similar current stress is experienced by all switching devices. Different voltage stresses are, however, seen. The output voltage and the voltage stress in S7 and S8 are identical. The input voltage and other switches are both under the same voltage stress. It should be noted that S7 and S8 endure higher voltage stresses than the other switches as a result of circuit asymmetry. As a result, selecting components requires tremendous caution.

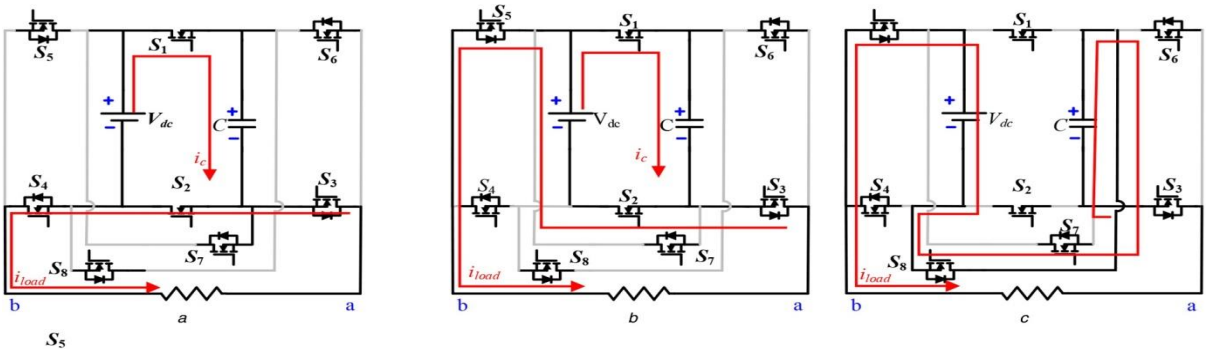
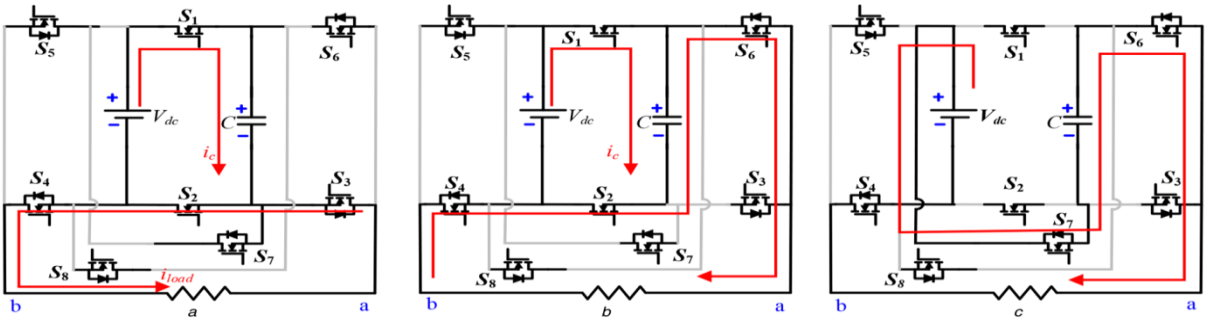


Fig. 3 (a) Mode I, Mode II, and Mode III are the operational modes.



Modes IV, V, and VI are as follows:

Fig. 4 operating modes

PWM is frequently used to operate power converter switches (dc or ac converters) at a predetermined switching frequency.

III. LEVEL SHIFT PULSE WIDTH MODULATION

The perpetration of the PWM block's palpitation pattern has resulted in an advanced modulation indicator and a lower harmonious profile of the affair waveform. Similarly, the design of modulation methods can reduce switching losses, current ripple, and capacitor voltage balance. The switching pattern of the switches in the two-position motor is developed by comparing a single triangular carrier with the modulation signal.

Table-II

Devices voltage and current stress

Device	Voltage stress	Current stress
$S1$	V_{in}	I_{in}
$S2$	V_{in}	I_{in}
$S3$	V_{in}	I_{in}
$S4$	V_{in}	I_{in}
$S5$	V_{in}	I_{in}
$S6$	V_{in}	I_{in}
$S7$	V_o	I_{in}
$S8$	V_o	I_{in}

The phase-modulated signal is compared to other topologies in order to build a similar approach with multiple topologies triangular carriers.

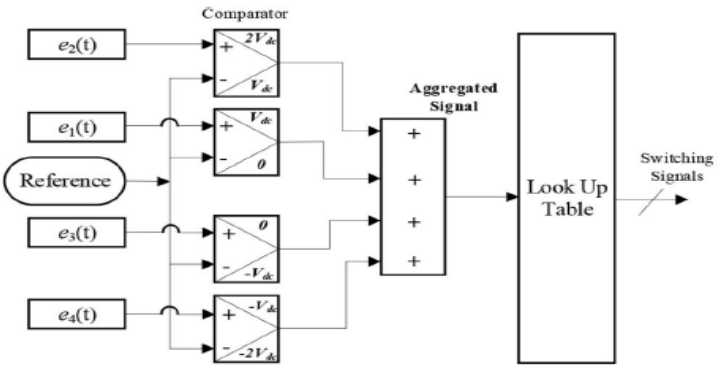


Fig. 5 shows a schematic for producing switching signals.

The two types of multicarrier modulation are phase-shifted PWM carrier and LS- PWM carrier, depending on the carrier arrangement. The five-position inverter proposed in this study is controlled using LS- PWM. Figure 5 depicts the general layout for producing switching signals for inverter switches. According to, an N-position inverter requires (N1) carrier waveforms and a reference signal. Because the proposed topology includes five situations, as shown in Fig. 6, four carriers are used. A sinusoidal reference is used to compare the carrier signals. In terms of waveform, the pattern of switching is recognized their phase shifts, amplitudes, and switching frequencies, all four carriers are symmetric. Four separate sectors are present due to modulation. At the launch of member 1, the carrier signal e3 is compared to the reference signal, resulting in an affair voltage ranging from zero to Vdc. Sector 2 generates affair voltage ranging from Vdc to 2Vdc by comparing the reference signal with the carrier signal e4 due to the symmetrical operation of the

proposed seven-position boost motor. In an analogous manner, the positive half cycle is demonstrated. Figure 7 depicts the switching patterns of a multilayer inverter.

IV. LOSS ANALYSIS

Switching losses happen when a switching device is switching, and conduction losses happen while a switching device is conducting (change state from off to on and vice versa). There are at least three switches that are either on or are being flipped to be on in each of the eight shifting stages. This leads to conduction and switching losses. The sections that follow discuss analytical calculations for switching and conduction losses

A .Conduction Losses

Two power switches that are unidirectional conducting and blocking and six additional switches that are unidirectional blocking and bidirectional conducting make up the eight switches in the suggested topology. The instantaneous conduction losses of the power switch and its body diode are given.

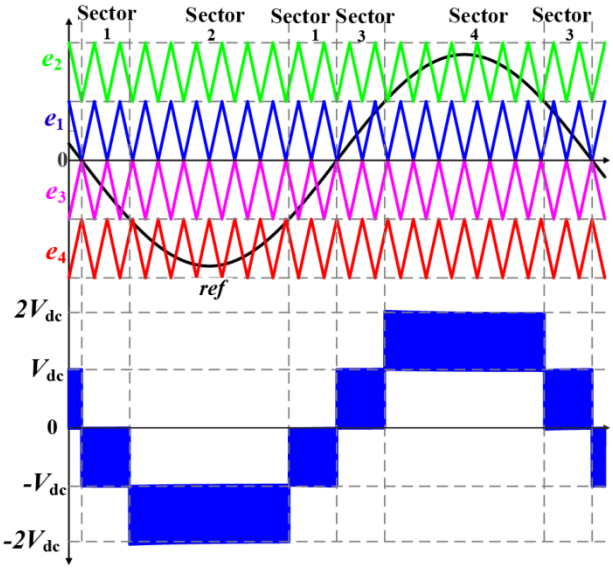


Fig. 6 LS-PWM scheme

$$\rho cT(t)= V +Ri^{\alpha}(t)i(t) \quad (5)$$

$$\rho c,D(t)= VD+RDi(t)i(t) \quad (6)$$

The average conduction losses are expressed as

$$\rho_{c.avg=\frac{1}{\Pi}\int_o^{\Pi}\left[\begin{matrix}\{N_T(t)V_T+N_D(t)V_D\}i_L \\ +\{N_T(t)R_T i_L^{a+1}(t)\}+\{N_D(t)i_L^2(t)\}\end{matrix}\right]d(wt)} \quad (7)$$

where c,T(t), c,D(t), VT, VD, RT, RD,, ND, NT where c,avg(t) represent the voltage drop in the on-state of the transistor, the simultaneous conduction losses of the transistor, and the diode voltage drop in the diode's on-state, the transistor equivalent on-resistance and the diode equivalent.

B. Changing losses

The voltage and current during the switching time are approximated linearly can be used to compute the switching losses of any switching device [14, 24].Calculations of turn-on energy loss consist.

$$E_{on.j} = \int_o^{t_{on}} \left\{ \left[V_{o.j} \frac{t}{t_{on}} \right] \left[-\frac{I}{t_{on}} (t - t_{on}) \right] \right\} dt = \frac{1}{6} V_{o.jIt_{on}} \qquad (8)$$

In a similar manner, the jth switch's energy losses during turning off are calculated as

$$E_{off.j} = \int_o^{t_{off}} \left\{ \left[V_{o.j} * \frac{t}{t_{off}} \right] \left[-\frac{I}{t_{off}} (t - t_{off}) \right] \right\} dt = \frac{1}{6} V_{o.jIt_{off}} \qquad (9)$$

Namely, Ton, I, Eon, J, and J Vo The turn-on voltage, turn-off current flow, turn-off duration, turn-off loss, and turn-off loss for the jth switch are denoted by the terms Eoff,j and toff, respectively. Here is how to determine total switching power losses:

$$\rho s = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{o.j} * I(t_{on} + t_{off}) f_j \right] \qquad (10)$$

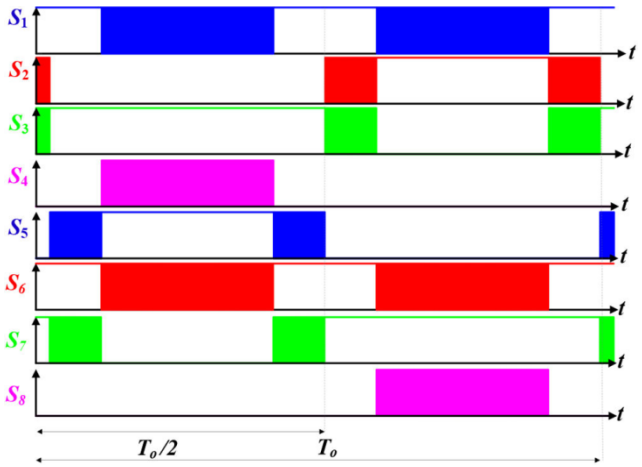


Fig. 7 displays the signals that operate the five-position inverter

The proposed inverter's ideal working power range is 350 to 650W. However, it is less effective than 95 in every power range up to 800 W.

V. SIMULATION RESULTS

To evaluate the functioning under various circumstances, a simulation is constructed in the lab and the system is simulated in MATLAB/Simulink.

A. Results from simulations

The input voltage and switching frequency are both fixed at 200 V and 5 kHz respectively during the simulation. Several study scenarios have been investigated using the simulation platform. In Fig. 8, the simulation model is shown. It should be noticed that an inrush charging current happens each time the capacitor C is charged. In Fig. 12, this behaviour may be seen. The suggested topology is therefore better suited for low power applications.

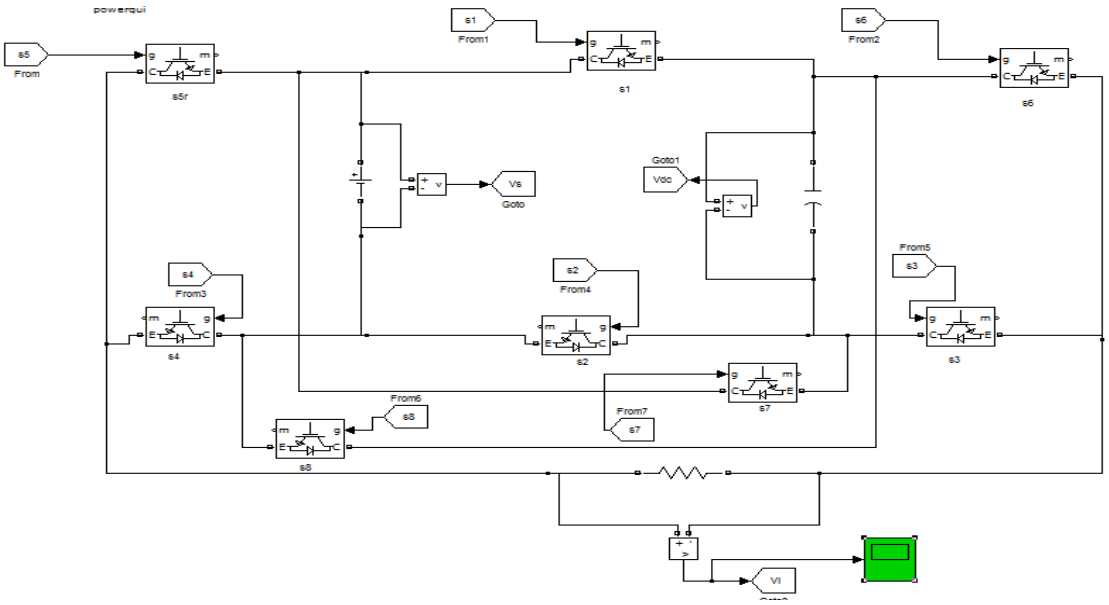


Fig. 8 Simulation model

The suggested arrangement only contains one DC source and one capacitance. This topology performs significantly better than other topologies mentioned in the literature since no equalisation management is required. The connections between an electrical converter, an output filter, and a resistive load are shown in Figure 8. The output voltage, also known as output current, has five levels (0, VDC, 2VDC, - VDC, - 2VDC).

Figure 13 displays the approximately 6% total harmonic distortion (THD) for this research scenario. Since the suggested topology only has one capacitor and one dc source and does not need for balancing management, it clearly outperforms other topologies in the literature without utilising an output filter, the inverter's related resistive load in Fig. 8.There are five levels of voltage and output current available (0, vdc, 2vdc, vdc, 2vdc). According to the findings of this investigation, the total harmonic distortion (THD) is about 6%, as shown in Fig. 13. In contrast to two-level or three-level systems, this number could be decreased to a standard value after the addition of a filter with a modest filter size.

As a result, the planned architecture is better suitable for low-power applications.

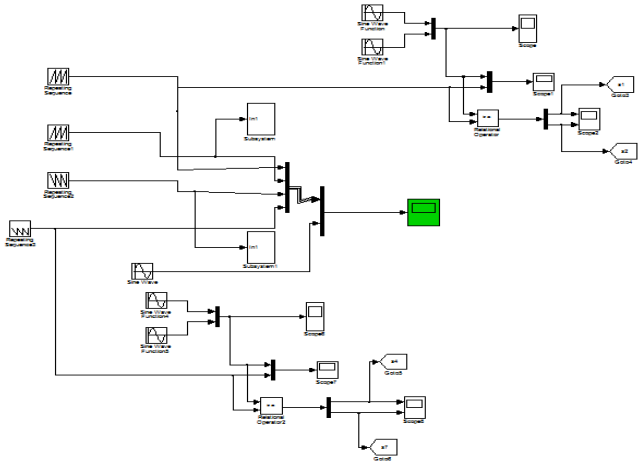


Fig. 9 switching circuit

This value can be simplified for lower filter sizes after the addition of a filter in comparison to 2-layer or 3-layer designs. In this case study from Associate in Nursing, a resistive load is connected to an electrical transducer terminal. Even in the absence of an output filter, as is the case with resistive loads, the resistive load smooths the output current. The output current degree, which is approximately 5.14%, is shown in Figure 12.

The aforementioned circuit was created using signal blocks in Matlab/Simulink, and a dc source served as the system's input. An IGBT switch and a multilayer inverter were used to construct the circuit.

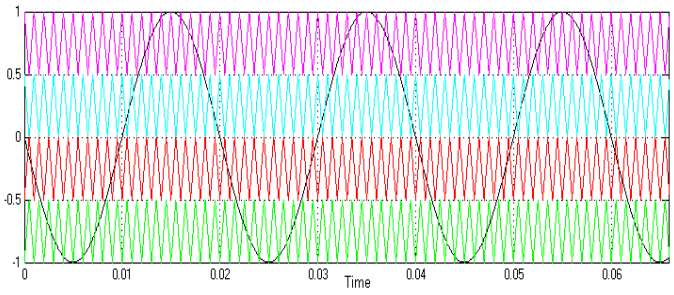


Fig. 10 shows the sine wave's carrier signals.

The THD of the output current is consequently decreased to 8%. The five-level boost inverter that is proposed is compared to various five-level topologies that are mentioned in the literature in Table 3. Since the NPC would require eight power switches and five capacitors without boosting capability, the output voltage would be lower than the input voltage. There are the same amounts of components in the FC five-level inverter as in the NPC, however there are only three rather than five capacitors.

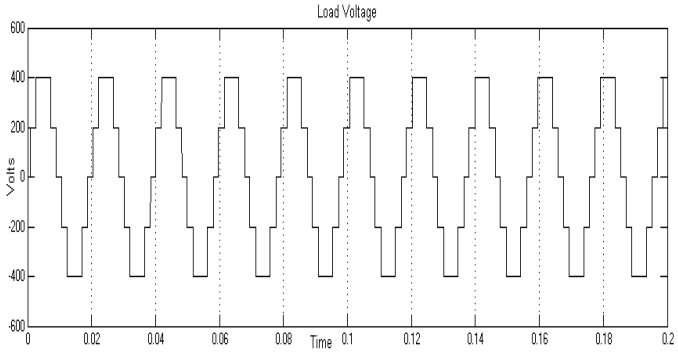


Fig. 11 shows the output voltage with a resistive load (R = 10 and L = 5 mH).

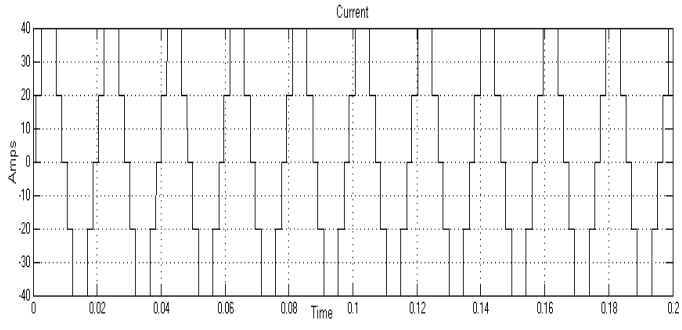


Fig. 12 Current waveform

Component specifications for single-phase multilevel inverters with five levels Figures depicting output five-level voltage and currents are shown above (11&12) take a look at figure 11 to see how the suggested multilayer inverter doubles the input voltage at the output. Component requirements for five-level, single-phase, multilevel inverters The output five-level voltage and currents are shown in the aforementioned figures (11&12) The proposed multilayer inverter doubles the input voltage at the output, as shown in figure 11.

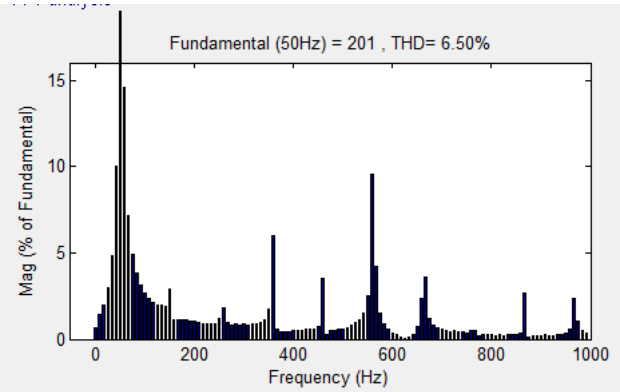


Fig. 13 THD of output voltage

Table-III
Component requirements for single-phase five-level multilevel inverter

Topology	NPC [34]	FC [19]	CHB [35]	Capacitor clamped [38]	Proposed
No. of Switches	8	8	8	12	8
No.of Diodes	0	0	0	0	2
No. of capacitore	3	3	0	4	1
No. of dc sources	1	1	2	1	1

Capacitors are not needed for the CHB inverter, but numerous unique dc sources are.

VI CONCLUSION

This study presents a multilayer inverter with five boost levels. The single-phase variation's manufactured configuration consists of eight switches and a dc capacitor. It can deliver a five level output with an output amplitude larger than double the input voltage. The balance issue is unimportant in this design because there is just one capacitor employed. Due to its growing potential, the suggested inverter is a competitive choice for PV system applications. The DC source charges the DC capacitor, which is then reconnected in series with it. Hence, a higher output voltage is possible. It makes use of LS-PWM.

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