Turkish Online Journal of Qualitative Inquiry (TOJQI)
Volume 14, Issue 1, January 2023: 135-145

Modulation of a Bidirectional Buck-Boost Current-Fed Isolated DC-DC Converter

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Abstract- Isolated bi-direction DC-DC converters are frequently used for energy storage systems (ESS) of DC micro grids. There is particular interest in a current-fed isolated bi-directional DC-DC converter (CF-IBDC) because of its advantages, notably the inherently lower current ripple on the battery side. However, the conventional control techniques are not very effective under both light and severe load conditions. This paper suggests a hybrid switching modulation to boost the CF-power IBDC's conversion efficiency under both low and high load circumstances. Depending on the amount of power supplied, separate controls are used to adjust the phase shift angle and the duty cycles of the secondary sides. In order to optimize zero-voltage switching, the control mechanism relies on (ZVS) circumstances and lowers the power converter's circulating current. The suggested control technique uses a single phase-shift modulation (SPSM) Modulation optimization, bidirectional boost-buck conversion, and a current-fed DC-DC converter to provide ZVS capability under all load conditions and to reduce circulating current.

I. INTRODUCTION

Due to its benefits of good soft-switching operation, wide voltage conversion range, and other fundamentals, the bidirectional insulated DC-DC motor has developed in fashion ability and has a wide range of implicit operations in the domains of solid state motor, energy storehouse system, and other areas the additional [1,6]. The key item on the list of typical topologies that follows is the bidirectional insulated DC-DC motor. The first DC-DC motor grounded on is binary active ground (DAB). Theoretically, this topology is capable of extensive voltage conversion, long-distance power transmission, and full soft switching operation. Nonetheless, the high current stress is still its primary excrescence [7, 10]. Underutilizing the power switches' current circumstances and other factors cause the system's cost to rise. The alternative gadget is a DAB DC-DC motor with an energy storage tank made of an inductor and capacitor. Given its higher current ratio of 1.6 [11]–[16] and quasi-sinusoidal operational current waveform, this type of topology has better electromagnetic properties. These benefits over the DAB converter have led to the resonant-type DC-DC converter's widespread usein the intermediate or small power and low-voltage systems then when there is a very high voltage and a high voltage across the resonant capacitor. Moreover, as the power rating increases, the resonant capacitor's capacitance will increase [17]. It can be difficult to construct a non-polar capacitor with such a high voltage rating and large capacitance.

The current-fed isolated DC-DC motor (CFIDC) [18] is the third option [19]. The two topologies run very differently as a result of the configuration differences from the inductor-grounded DAB DC- DC motor. The average and maximum motor current values in the CFIDC are

theoretically extremely close to one another. It generates the most hardware power rating consumption when compared to the other two groups. The CFIDC is comparable to a regular if the motor current opposition reversal method is disregarded; boost the DC-DC motor. Hence, it is restricted to increasing conversion. Yet, due to the large friction of the terminal voltage of the energy storage components, many real-world operations, such as battery or super capacitor charging/discharging systems, require the charging/discharging system to be capable of wide voltage conversion range. It's shocking that this program's goal extends beyond simple conversion addition.

In this work, the development of Many application areas are made available by a bidirectional boost-buck CFIDC, which preserves the benefits of the CFIDC's quasi-unity current flow while widening the range of its voltage conversion. Moreover, the duty cycle of the buck unit and the shot through time of the H- ground motor are adapted by reducing the average inductor current. Also, the suitable duration of the rising edge of the power switch of the buck unit with respect to the beginning of the switching cycle is established by lowering the inductor current ripple. The benefits of the recommended topology are contrasted with a number of well-known DC-DC converters to show their superiority.

Below is an example of a bidirectional DC-DC converter based topologies have historically been increasingly supplanted by traditional silicon controlled rectifiers (SCR) switching power supplies with power ratings in the tens of kilowatt range. The advantages and disadvantages are both widely known. It is possible to use lighter and smaller magnetic components, and high frequency switching power supplies offer quicker reactions to line and load disturbances. Due to the demands placed on switching devices, the main disadvantage of high power switching power supply is that they are frequently less reliable than their SCR-based relative.

High-power switch mode applications today use a variety of power circuit topologies. Three steps of power conversion are used in the most typical configurations:

• A three-phase incoming mains voltage that an AC to DC converter transforms into a DC voltage.

• A DC to AC motor or inverter that converts the voltage on the DC machine into a high-frequency AC voltage;

• An alternative AC to DC motor that converts high-frequency AC voltage into DC voltage. The two AC to DC transformers run simultaneously, with the exception of the working frequency; they typically employ cures, low pass filters, and snubbers. The snubbers control parasitic element parasitic voltages and waste energy from switching flash voltages. The alternate stage's DC to AC motor generates a high-frequency voltage that typically operates a motor at a frequency of 20 kHz or fewer. It is vital to use ohmic insulation since the motor generates the high voltage, which is grounded on the motor turn’s rate.

The most difficult part of the process is the DC to AC converter, and various power processing topologies are now in use. Most high-power DC to AC converters uses an H-bridge architecture, which consists of four power devices, to excite the high-frequency transformer. The pulse width modulation (PWM) or other modulation techniques are used to control the H-bridge in order to supply a voltage with a restricted pulse width or amplitude.

A modulated H-bridge produces a changing output voltage. There are three different types of DC to AC converter topologies: resonant, soft-switched, and hard-switched. The load line on the switching device during commutation time is the primary distinction between the topologies (switching transition). Power devices waste the greatest power when switched to the "off" state. Hard-switched converters can be used by snubbers and/or power devices to capture commutation energy. To shape power waveforms and reduce losses during the commuting phase, soft-switched

transformers permit new, unresistive circuitry. The circuitry's complexity, advanced on-state losses, and susceptibility to loading conditions outweigh the advantages of lower dicker losses (resulting from waveform revision). Due to their well-tuned tank circuits, resonant power transformers appear to have sinusoidal device voltage or current. Same benefits and drawbacks apply to soft-switched transformers with second-order resonant power converters as opposed to soft-switched converters, timing is more crucial.

Due to the fact that they are primarily designed to operate off of a DC voltage supply, hard-switched, soft-switched, and resonant converters are commonly referred to as voltage-fed converters. Shooting difficulties, which can happen when one device in a series connection fails to turn off before the second item in the connection goes on, are common with voltage-fed converters. The protective circuitry should normally be able to identify shoot-through issues in one to two microseconds, despite the fact that protection circuits can be designed to prevent catastrophic accidents. Transformer core saturation may be caused by changes in device parameters and unusual voltage-fed converter modulation during the half-cycle. Before any damage is done to the power semiconductors, protective circuitry must be able to recognize these situations.

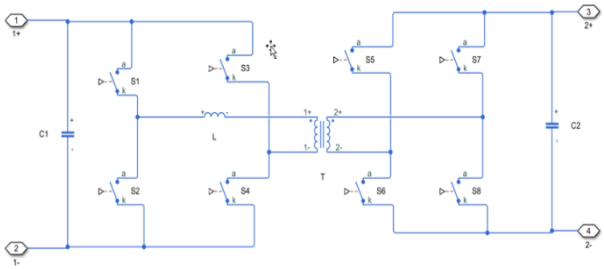


Fig.1 Converter with two active bridges

II. PROPOSAL SYSTEM

The recommended insulated DC-DC motor with bidirectional buck-boost current supply is shown in Figure 2. (B3CFIDC). It has one ground arm with switches S11 and S12, two H-ground transformers (HB1 and HB2), an inductor L, a high frequency insulation motor, two H-ground transformers (HB1 and HB2), and one ground arm (HFT). The HFT's leakage inductor (Llk) and winding rate (n) correspond to these numbers. A typical current-fed isolated DC-DC motor is made up of the corridor L, HB1, HB2, and HFT. When power is transferred from U1 to U2, just a buck operation and a boost operation are performed when the power is switched back the other way, are possible, according to [19]. When the power for the planned converter is switched from S12 to its equivalent circuit, S12 is shut off U1 to U2 (forward mode).

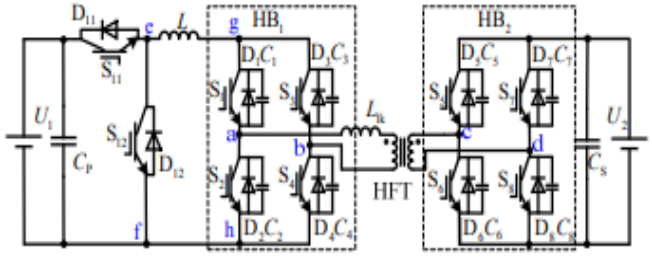


Fig. 2 Schematic of proposed B3CFIDC

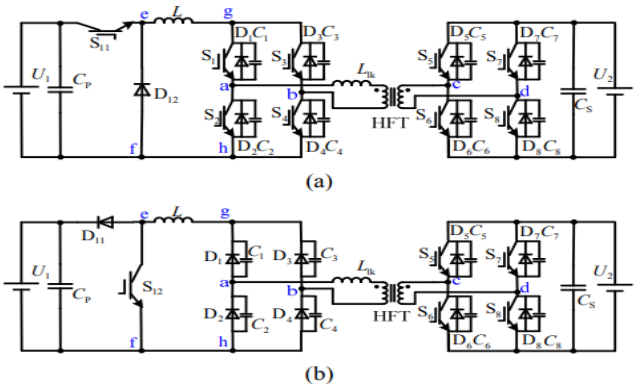


Fig. 3 Equivalent circuits in the two transfer directions of the suggested architecture are depicted (a) from U1 to U2 (forward mode) (b) from U2 to U1 (reverse mode)

In addition to the normal boost operation, the buck operation can also be carried out by modifying the forward mode of S11's work cycle (d11). Switch S11, whose circuit is similar to that in Fig. 3, turns off when power is applied in the other way (b). The recommended motor can run in boost mode by adhering to S12's duty cycle in rear mode. According to the aforementioned study, the proposed topology may provide buck-boost operation and bidirectional power transmission by integrating switches S11 and S12. To lay the groundwork, the suggested topology's operating principle is examined. See this section for details on the ensuing modulation technique and optimization plan. Due to space constraints, this research only looks at the forward mode's operational mechanism because the proposed topology's operating mechanism is dual for the two power transmission directions.

The forenamed circuit can operate in either buck mode or boost mode depending on how the Mosfets Q1 and Q2 are moved. The circuit modifies the voltage applied across the anti-parallel diodes D1 or D2 in a similar manner when switches Q1 or Q2 function as a footloose diode. The two modes listed below are the two directions in which the forenamed circuit operates.

Mode 1: The boost mode's first mode Switch Q1 and diode D2 are both permanently off in this mode. While the duty cycle determines when the diode D1 and switch Q2 start conducting. Also, based on the conductivity of the switch Q1 and the diode D2, this mode can be divided into two intervals. At the first interval, Q2 is on, D2 is off, Q1 is off, and Q2 is on. Q2 becomes active and is capable of being checked for short circuits when the lower voltage battery charges the inductor. The inductor current increases until Q2 and the gate palpitation have not yet been separated. Also, because switch Q1 is rear-poisoned and inoperative in this mode, no current passes through it.

Interval 1 (Q2-on, D2-off*;* Q1 off, D1 off, Q2 off, and Q3 on. With this configuration, both Q1 and Q2 are off. They could be thought of as open circuited. Considering that the current entering the inductor cannot. The voltage across the inductor now changes polarity instantly and operates with the input voltage in series. As a result, the diode D1 becomes contaminated and advances. The inductor current consequently charges the relationship capacitor C2 to a high voltage. As a result, the voltage of the affair rises.

***Interval 2 (Q1-off, D1-off; Q2-off, D2-on*)**: Switch Q1 and diode D2 work in accordance with duty cycle, whereas switch Q2 and diode D1 is always off. This mode can be split into two intervals using the conduction on the switch Q2 and the diode D1. In interval 1, Q1 is on while Q2 is off. (Q2 on, D2 off; Q1 off, D2 off) the inductor and the o/ p the high voltage battery will charge the capacitor.

Mode 2: During this interval, Q2 and Q1 are, respectively, both off. Due to the inductor current's inability to fluctuate continuously, it is now discharged via the free-floating diode D2. The voltage across the cargo is decreased in accordance with how the input voltage is connected. Here, the properties of the non-isolated bidirectional topologies are contrasted.

Interval 1 (Q2-on, D2-off; Q1-off, D2-Off): The RMS value of the current in the inductor and the power switches in the buck-boost bidirectional motor is advanced during step-up mode by a quantum that is equivalent to the increased current when compared to the buck-boost waterfall bidirectional motor. Moreover, the capacitor's 1/3 of the RMS current exceeds the specified current. So, when compared to the buck-boost cascade converter, the power switches, inductor, and capacitor in the bidirectional buck-boost converter operate under greater thermal and electrical strains, increasing power loss and inductor core saturation.

Interval 2 (Q1-off, D1-off; Q2-off, D2-on): The MOSFET and the diode are put under more strain Power bias with advanced device characteristics are therefore required in the buck-boost bidirectional motor. Moreover, larger RMS currents result in increased conduction a loss, which reduces the overall efficiency of the buck-boost bidirectional motor nonetheless, in contrast to the buck-boost.

A waterfall buck-boost motor needs twice as many components as a bidirectional motor. This problem can be solved by using a bidirectional DC-DC motor with half-grounding. It can be used in place of the buck-boost waterfall bidirectional motor for activities that only bear boost action in one direction and buck operation in the other. The number of biases is the same 3. The half-ground bidirectional motor offers several benefits over the bidirectional Cuk motor, including the requirement of just one lower inductor. The half-bridge converter is more efficient than the Cuk converter due to lower input current and lower conduction and switching losses.

The suggested converter's performance is evaluated for the operational waveforms shown in Fig. 2.6 at each period. [t0, t1): During this time, iL travels via D12 while S11 remains in an off state. D6 and D7 supply secondary HFT input current to U2 for use in the HFT through the on-stated S2 and S3 of HB1, which are also in the on state. The inductor L can be thought of as a current source that moves power from the primary side to the secondary side of the HFT since U1 doesn't generate any electricity. In addition, iL gradually deteriorates while nU2 operates. (t1, t2) At time t1, S1 and S4 become active, and C1 and C4 begin to discharge. Voltage grows quickly as it decreases from U2 to zero. When uab hits zero at time t2, the motor current increases due to the action of U2, and as a result, iL and strain are no longer equal. KCL regulation states that at zero, the current flowing through S1–4 starts to grow. t2, t3). The two ground arms of HB1 are both fully extended at t2, when S1- 4 is fully engaged.

iL passes through D12 and both of HB1's bridge arms. L doesn't lose any voltage, so iL doesn't change. In Fig. 3, the voltage across Llk is shown. As a result of U2's performance, it starts to increase. As of now, there are currents flowing via the power switches on HB2.

$$u_{ik} = u_{ab} - nU_2 \approx -nU_2 \qquad (1)$$

So i_{lk} can be approximately expressed as

$$i_{ik} = -i_L + nU_2(t - t_2)/L_{Ik} \qquad (2)$$

Starting at zero, Although the currents through S2 and S3 start to decline, those via S1 and S4 start to climb. Each switch's instantaneous current in HB1 is provided as

$$i_{s2} = i_{s3} = I_L - nU_2(t - t_2)/2L_{Ik} \quad (3)$$
$$i_{s1} = i_{s4} = nU_2(t - t_2)/2L_{Ik} \quad (4)$$

[t3, t4):At time t3, Ilk reaches zero. When S2 and S3 currents decrease to IL/2, S1 and S4 Currents reach an IL/2 level. Since the S1-currents 4 and ilk are both constant, all of HB2's power switches are in the off position. When frequency is reduced, D6 and D7 on HB2 are silently turned off. As can be seen in Fig. 3, this time frame is referred to as the break S d T. [t4, t5]: U2 is applied to the 0 at time t4, at which point the secondary side of HFT starts to rise. At the same time, S6 and S7 are turned on because abu deviated from zero due to the influence of U2. As a result, S2 and S3 currents start to rise while S1 and S4 currents start to climb from IL/2 start to diminish from

$$i_2 = i_{s7} = i_{s6} = ni_{Ik} \quad (5)$$

[t5, t6):Time t5 sees the activation of S11, followed by the application of U1 to the zero and the expression of inducer L. Because uab=0, the expression for iL is valid.

$$i_L = i_L(t_5) + (U_1 - U_{ab})(t - t_5)/L = i_L(t_5) + U_1(t - t_5)/L \quad (6)$$

Due to the fact that L is substantially larger than Llk, the rising rate of Li is significantly smaller than the rising rate of Llk. The energy from U1 is stored in L.

[t6, t7]At time t6, the currents flowing through S1 and S4 whereas the currents passing through S2 and S3 decrease to nil, they increase to IL. Lk I also a scends to IL at this time. There are two directions in which the LK current moves. As the other travels from D2 to S4, one journeys from S1 to D3. For currents flowing through HB1, the equation is

$$i_{D2} = i_{D3} = 0.5(i_{Ik} - i_L) \quad (7)$$
$$i_{s1} = i_{s4} = 0.5(i_{Ik} - i_L) = 0.5i_{lk} \quad (8)$$

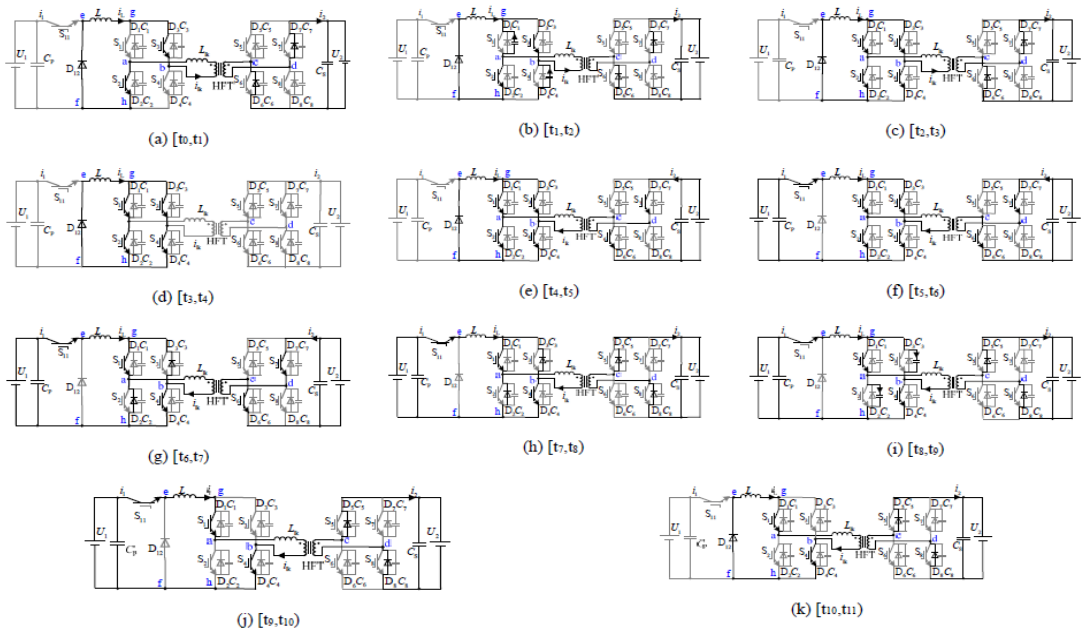


Fig.4 shows equivalent circuits with various intervals.

[t7, t8):S2, S3, S6, and S7 are all inhibited at t7. Zero-current switching (ZCS) is used for S2 and S3 because there is no current flowing through them. Abu deteriorates over time, therefore. It implies that lk I, also known as lk max I achieves its maximum at time t=t7. In order to prevent

voltage spikes throughout the whole power range, the rated inductor current L rate I and I should be taken into account when designing lk max I. As a result, lk max I can be used to determine the expressed current margin lk.

$$i_{lk\_max} = I_{L\_rate} + \Delta i_{Ik} \quad (9)$$

When lk I begins to diminish, the currents via S1, S4, D2, and D3 also begin to decrease. As a result, one may determine the current stress of each power switch using equation (7) -. (9).

$$i_{D1-4} = i_{s1-4} = I_{L\_rate} + 0.5\Delta i_{Ik} \quad (10)$$

The secondary transformer current also passes via D5, U2, and D8 before arriving at D8. It shows that the converter is operating in its usual power transfer mode. Likewise, [t7, t8duration]'s

$$d'T_s = (I_{L\_rate} + \Delta i_{Ik} - I_L)\, L_{lk}/nU_2 \quad (11)$$

$$i_L = i_L(t_9) + (U_1 - nU_2)(t - t_9)/(L + L_{lk}) \quad (12)$$

[t10, t11):The inactivation of S11 and the start of iL flow through D12 occur at time t10. The condition of iL begins to decline at a rate of 2 lk ()/() nU L L. The relationship between Next, the under control variables (d11, d, and ds), the independent variable (IL), and the voltage conversion ratio (k=nU2/U1) are looked at. In Figure 4, the letters Uef are used to represent the average voltage between points e and f, while Ugh are used to represent the average voltage between points g and h. Because it is possible to rectify the uab waveform in Fig. 4 to obtain the waveform of the instantaneous voltage between g and h, calculating the average value of uab over the period of a half switching cycle will result in Ugh. It is possible to express the two average voltages as

$$U_{ef} = d_{11}U_1 \quad (13)$$

$$U_{gh} = 2(1 - d - d')nU_2 \quad (14)$$

At steady state throughout the half switching cycle, the volt-second product of L is 0. It suggests

$$U_{ef} = U_{g1} \quad (15)$$

The voltage conversion ratio and the controllable variables therefore have the following relationship:

$$k = n\frac{U_2}{U_1} = \frac{d_{11}}{2(1-d-d')} \quad (16)$$

When (11) is put into (16), k is represented as

$$k = \frac{d_{11}}{2\left[1-d-L_{lk}\left(I_{L\_rate}+\Delta lk\right)-I_L\right)/nU_2T_s]} \quad (17)$$

According to (16), by concurrently changing d11 and d, the converter > 0.5 and d'0 can conduct the boost and buck operation.

III. MANAGEMENT STRATEGY FOR PROPOSED OPERATING MODE

In line with the load conditions, Fig. 5 displays the phase voltage and phase voltage waveform under various control modulations. The light load state in Figures 5(a) and 5(b) results in a high peak current, which raises core loss and conduction loss. Using the PPDPS with the fixed Zd in Fig. 5-(c) as an option can lessen power loss, despite the fact that the high peak current duration in this composition only ends when PS reaches Zd/ 2. The circulating current of the phase current, which is caused by the zero vectors of the HVS, is seen in the darkened area of Figure 5. According to Fig. 5, the suggested control method for the HL mode reduces the circulating current using the PPS approach (d). The PPS design may minimise circulating current and reactive power in contrast to Figs. 5-(e) and 5-(f) because it may avoid the zero-vector on the HVS under the heavy cargo script (f). While the PPDPS is in use, the non-power transmission zone grows as power increases, as depicted in Fig. 5. (e).

Even though the zero-vector on the HVS is continuously maintained, the PPDPS with the fixed Zd encounters the same issue with the heavy cargo script depicted in Fig. 5-(f). Figure 5 shows the phase voltage and current waveforms for the following operation modes. PPS with light loads is illustrated by PPS, PPDPS, and PPDPS with fixed T. PPS under a large cargo, PPDPS with fixed T under a heavy cargo (f), and PPS with a heavy cargo (e) (d).

Using the fixed Zd with PPDPS is therefore only appropriate for light loads. The ML mode acts as a transition from the LL mode to the HL mode. It is able to go seamlessly from the PPDPS with a fixed Zd in the low freight state to the PPS control when power increases because the PWM of D2 is only utilised to control the affair power in the ML mode implementing a simple control approach. The CF- IBDC control demonstration based on the recommended system is shown in Fig. 6. Both a setting voltage control circle (Gvc(s)) and an affair voltage control circle (Gvo(s) & Gi(s)) must be created as control circle regulators.

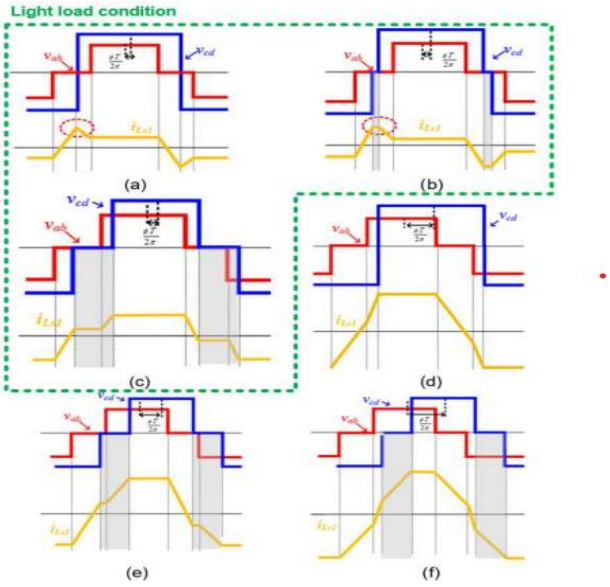


Fig. 5 Phase voltage and current waveforms under operating modes: (a) PPS at light load, (b) PPDPS at light load, (c) PPDPS with fixed ΔT at light load (d) PPS at heavy load, (e) PPDPS at heavy load, and (f) PPDPS with fixed ΔT at heavy load

The reference for the inner control loop is the output of Gvo's (the outer control) loop. PS and D2's control variables are independently regulated by the ZVS operation, the simple control approach, and the circulating current minimization.

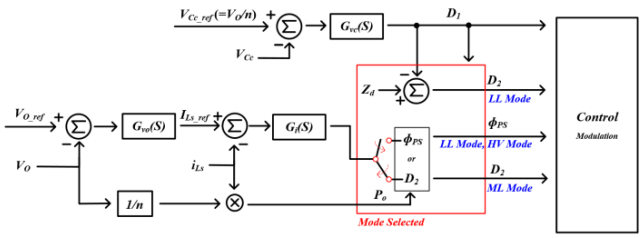


Fig. 6 shows the suggested current-fed bi-directional DC-DC converter's control scheme.

IV. SIMULATION RESULTS &DISCUSSION

A simulation is created, as shown in Fig. 7, to assess the fundamental performance of the suggested B3CFIDC and the optimised modulation technique. An adjustable resistor acting as the load is attached to a DC voltage source on each of the two DC sides of the B3CFIDC.

First, it is assessed how delicately the proposed topology's buck and boost operating functions are expressed in terms of the derived voltage conversion rate expression. The most effective control method is used by the modulation system. U1 is adjusted to 50V and 150V independently to verify the performance over a broad voltage conversion range. The predicted value of U2 is set to 200V on a separate DC side, and the load is a pure resistor. To further validate the suggested topology and theoretical analysis in boost and buck operation conditions as well as under colourful power situations, two essential reference powers are set. U1 is Each had initial settings of 150V and P 437W. The resistance R2 is changed to the appropriate value when the output power surpasses the reference power, causing U2 to theoretically equal 200V. According to the formula for the voltage conversion ratio, D should be where it is since the location is in buck operation, where the lowest allowed value is 0.55, and d11 should be 11 d 0.5835.

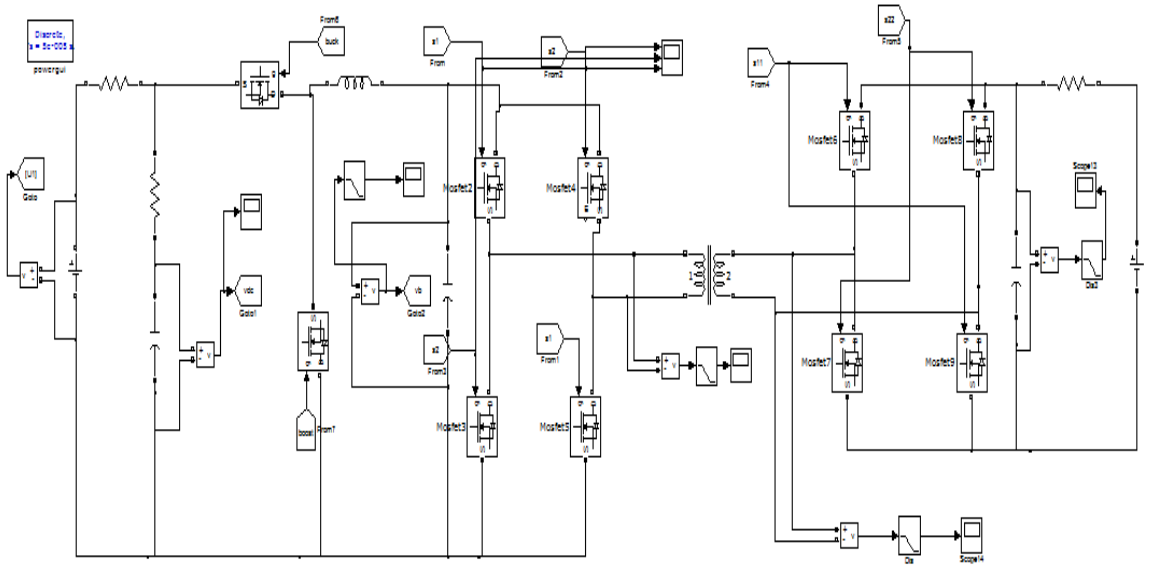


Fig. 7: Simulation of a circuit

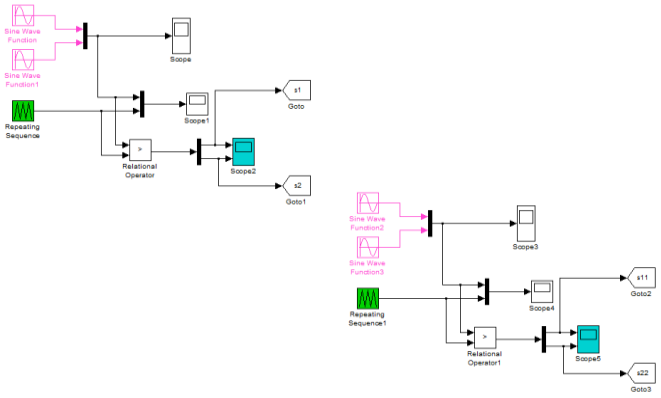


Fig. 8 shows the command system.

The proposed circuit was built using input dc sources, input power electronic switches (IGBT, Thyristors), and Matlab/Simulink. In Figure 8, it is shown. The proposed model separates the input from a dc source block using a transformer before passing it to the first half bridge by using Simulink source and signal blocks in Matlab (HBT).

Simulation results

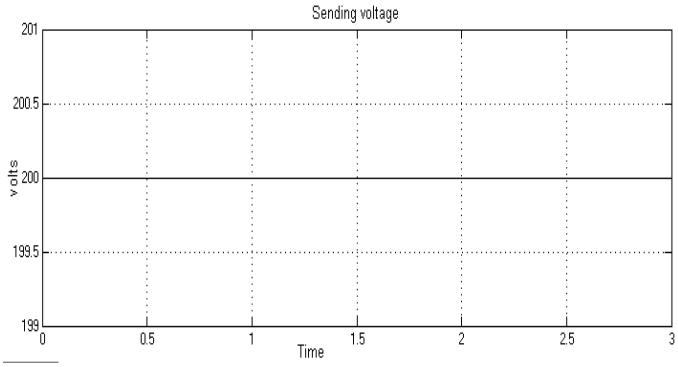


Fig. 9 Sending input voltage

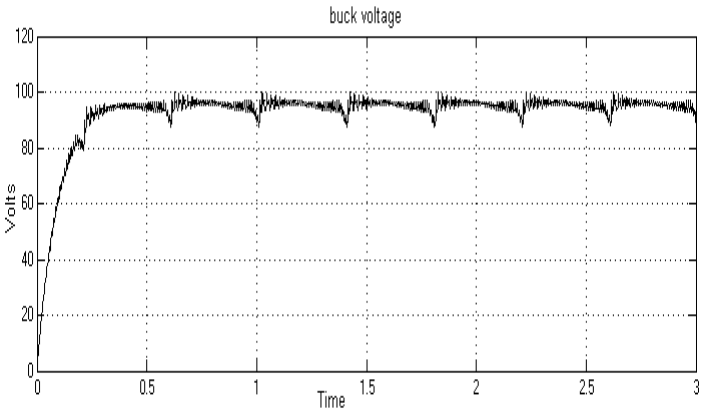
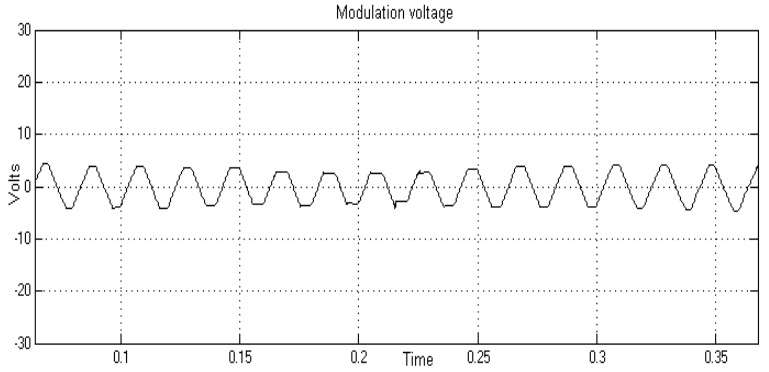
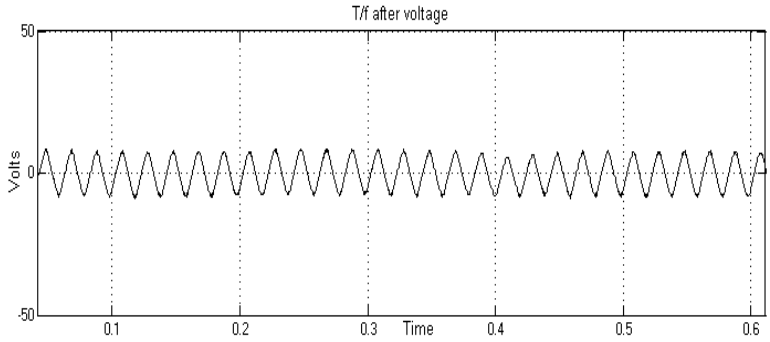


Fig. 10 Step-by-step voltage rise

According to figures 9 and 10, the input supply and buck-boost converter step-down the input dc voltage



(a)



(b)

Fig. 11The primary side and secondary side voltages of the transformer (a) and (b) above

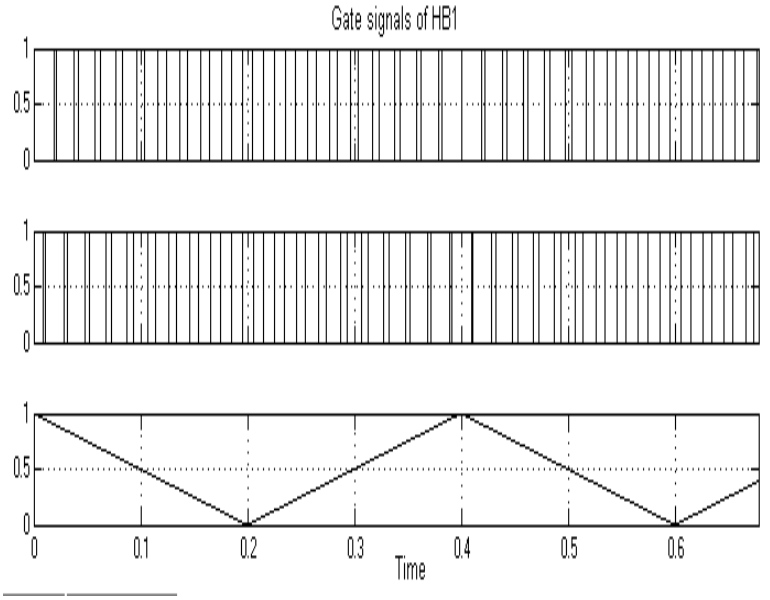


Fig. 12 shows gate signals

The pulse signals of the recommended HBT converters are shown in the figures above. The output signal of HBT is generated by two hall bridge techniques.

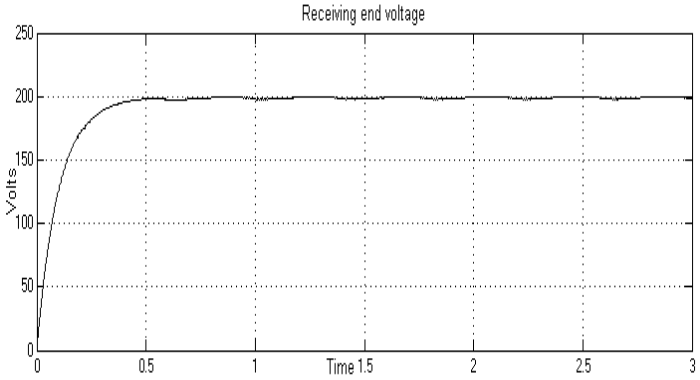


Fig. 13.Receiving end voltage

The advantages of the proposed topology in terms of voltage conversion range, current stress, and cost are further illustrated by comparisons to the conventional voltage-type dual active bridge (DAB) based DC-DC converter, the LC series resonant DC-DC converter, and the boost current-fed isolated DC-DC converter. The pertinent comparison information is shown in Table I. Peak-to-average current ratios are roughly 2 for DAB converters, 1.6 for LC resonant converters, and 1 for current-fed converters. For current-fed converters, the peak-to-average current ratios are typically about 1.

Table I
Data from Various Bidirectional Dc-Dc Converters

	DAB	**Resonant**	**Current-fed**	**Proposed**
Voltage conv. range	Buck-boost, wide	Buck-boost, wide	Boost, narrow	Buck-boost, wide
Current stress ratio	2	1.6	1	1
Number of switch	8	8	8	10
Number of equivalent switch	16	12.8	8	10
Cost ratio of switch	1.6	1.28	0.8	1

By dividing the actual number of switching devices by the current stress ratio, one can calculate the number of comparable power switches. The amount of similar power switches and the cost ratio are determined under the same transfer power in accordance with the present rating's roughly proportionate relationship, which simplifies the comparison. Table I demonstrates that, as compared to DAB and LC resonant DC-DC converters, the number of equivalent power switches of the suggested topology is reduced by 50% and 28%, respectively, at the same power. Contrast this with the boost current-fed DC-DC converter's greater voltage conversion range. Thus, the suggested topology offers outstanding all-around performance.

V. CONCLUSION

This research offers a helpful hybrid switching modulation to get beyond the limitations of the current control method and boost the effectiveness of power conversion under heavy load conditions, under CF-light IBDCs. A fixed Zd and a DC-filter constructed using a theoretical study can ensure the full ZVS range under low load situations. In order to reduce circulating current and reactive power, the duty cycle of the secondary sides is changed in line with the load conditions. The proposed hybrid algorithm, which can facilitate control, also controls the phase shift angle

between the primary and secondary sides and the secondary sides' decoupling duty cycle. A 1 kW CF-IBDC prototype operating between 48 and 60 volts validates the efficacy of the suggested hybrid control technique at 380 V of Vout of Vbat. The ZVS requirements of the power switches are verified using the two-pulse testing. Both the steady-state functioning and the dynamic response witness to the efficacy of the suggested control algorithm. According to test results, the recommended hybrid algorithm is more effective than the conventional control algorithms in light and heavy load settings by 3.3% and 1.8%, respectively. It is shown that the suggested switching pattern is effective.with the highest efficiency obtained at 800 W under Vbat = 60 V at 96.67%.

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