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Research Article

Implementation Of Reversible Logics On Combinational Circuits For Optimum Performance

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Abstract

In recent years, reversible gate has emerged as most exciting research mission for least power loss circuit design, with applications towards low power CMOS, cryptography and image processing .Also in nanotechnology, this proposal introduces a novel and quantum cost effective reversible complete adder circuit . This gate which is proposed is used as a reversible complete adder device on its own. It isverified that the proposed gate has less hardware configuration than its current counterparts.The researchers' theoretical minimum is also met by the proposed reversible multiplier.In comparison to the previous design, the new design has shown to be more successful.

1. INTRODUCTION

VLSI can be briefed as processing of combined numerous number of MOStransistors into a single chip Integrated Circuit (VLSI). As MOS integrated circuit chips were commonly used in the 1970s, complicated semiconductor &communication technologies could be evolved. VLSI systems are the microprocessor and memory chips.

At the beginning semiconductor chips had 2 transistors. As technology progressed, more transistors were introduced, and more functions were integrated over the years. The integrated circuits contains only limited components , briefly 10 diodes , resistors , capacitors and transistors , which allows more than one logic gate to be built on one board. Development in semiconductor technology has driven towards vast number of logic gates also called as MSI . Further advancements resulted in large-scale implementation.

Large-Scale Integration (LSI), which consist of combinations of at least a thousand logic gates.

At present, there are more than millions of gates and transistors, far surpassing this milestone.Once upon a time, there was a drive to mark and calibrate various levels of large-scale integration.There were two concepts used: Ultra Large Scale Integration (U-L-S-I) and Ultra Large Scale Integration

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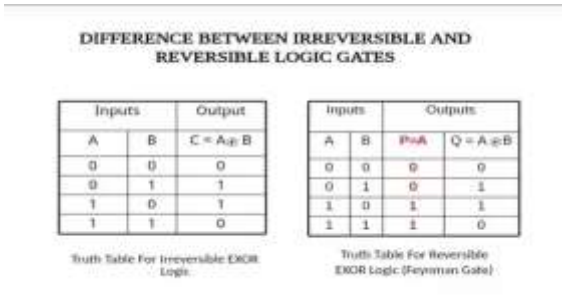
(U-L-S-I).Such fine distinctions are no longer valid due to the common availability of million gates and transistors on general` devices. Terms implying higher standards of integration than VLSI are not used further.Semiconductor device which can amplify electrical signal is known as a transistor. A transistor is a mandatory component of any latest technological device. Semiconductor materials have at least three connecting terminals. The current through another pair of terminals is regulated by a voltage or current applied to one pair of transistor terminals. Since the controlled (output) power can be greater than the controlling (input) power, a transistor can amplify a signal.Today, only a few transistors are packed individually, but many more are found in integrated circuits.

Conductivity of electricity in a semiconductor material isin the likes of a conductor, which includes metallic copper, and an insulator, like glass. The resistivity of a material depletes as the temperature arises - metals behave in the different way. By adding doping to the crystal like structures, its property of conduction can be changed in meaningful ways. Two differently doped regions in the same crystal leads to semiconductor junction formation. Latest electronics are made on the action of the charge carriers which includes electrons, ions, and electron holes .

Silicon,gallium arsenide, germanium and elements in the periodic table's "metalloid staircase" are examples of semiconductors. Second most common semi conductor which is gallium arsenide after silicon, and it's used also in things like solar cells, laser diodes and microwave frequency IC. Silicons are crucial components in production of most electronic devices.Semiconductor circuitshas lot of important applications, which includes the power to transfer current quickly in same direction over the other, variate the resistive property, light or heat sensitive property. Devices made of semiconductors are used in as amplifiers, switches, and energy conversion devices since properties of semiconductor material is generally changed by doping .Digital signal processing, networking, computer graphics, and cryptography all use reversible or information-lossless circuits. In addition, they are in the new field of quantum computing, there is a fundamental necessity. If we examine the synthesis of reversible polymers, we require circuits with a small specifiedquantity of gates and a small quantity of transistors. There is no redundant input-output line-pairs in the system. Quantum computation cannot be realised unless reversible logic is applied. The primary aims of reversible logic architecture are to lower quantum costs..The number of garbage outputs and the depth of the circuits. A fault tolerant reversible logic has gained significance as they consume low power and less heat dissipation. In irreversible logic for the possible outputs, we have distinct input combinations but don’t know the exact location of the inputs. By implementing reversible logic, we can trace the input information using the garbage output. The major difference is reversible gates don’t lose input information whereas irreversible gates do loose some significant amount of information. Only by using physical reversibility will you benefit from logical reversibility. To save electricity, any future technology will have to use reversible gates.



Reversible computing is a computational paradigm in which the computational mechanism is partially time-reversible.The mapping from states to their successors must be one-to-one, which is a necessary requirement for reversibility in a model of computation that uses deterministic transformations from one state of the abstract machine to another. Reversible computing is a form of unorthodox computing that requires a deep understanding. In irreversible logic for the possible outputs, we have distinct input combinations but don't know the exact location of the inputs. By implementing reversible logic, we can trace the input information using the garbage output. The major difference is reversible gates don't lose input information whereas irreversible gates do loose some significant amount of information. Traditional combinational logic design techniques are vastly different from reversible logic design. Garbage outputs are output lines that are never used again.Reducing the trash is one of the most difficult task .

A reversible gate can realise reversible operations only. Several Boolean functions, on the other hand, are immutable. Before we can grasp those factors, one must first convertconventionaloperations into reversible operations. Any conversion algorithm that changes aconventional feature to a reversible operation adds lines which give input are set to 0 on the input hand. They are referred to as constant inputs.

As a consequence, good reversible logic architecture must strive to minimise all garbage and persistent inputs.Since reversible circuit input vectors may be uniquely extracted from their corresponding output vectors, reversible logic naturally handles heating. This proposed design can then be implemented in a variety of processors for maximum performance. This paper proposes the design of a multiplier circuit with the fewest transistors required, consisting of a complete adder and only reversible logic gates. Technological advancements have allowed the incorporation of billions of transistors on a single die, providing designers with the flexibility and ability to add more features into the same die. As a result, there has been an uptick in power demand, which has resulted in the development of a slew of new techniques to deal it.

Since conventional computing is eternal in constant, the circuit's input and output cantbe calculated. Single bit of detail is dissipated in a OR process, for exampleLandauer showed in 1961 that, if mechanical considerations and processing materials are neglected, a digital circuit's energy consumption is largely attributed to the conventionality of the functions performed . It is demonstrated that K*T*ln2 (K-constant, Boltzmann's constant) joules of heat are lost for any bit dissipiated during conventional processing of information. Bennet went on to state that if reversibility is built into computing, the processing will not be limited by the one mentioned in so no information will be lost. Since each state transition is reversible, the logical states are thermodynamically identical, resulting in least heat dissipation. Bennett showed that reversible logic has no major power loss and no data leakage. According to latest studies, the usage of reversible gates in logic circuit design has increased significantly.

QCA (quantum dot cellular automata) is a novel nanotechnology with limited feature sizes, large clock speeds, and very low power consumption. QCA is a novel method of computation in which

the electron locations decide the logic states ("0" and "1").Because of the high error rates, maintaining incredibly low system error rates in nanoscale production and nanotechnologies, like the QCA, is important. Defects can occur during the QCA manufacturing processes of synthesis and deposition. In contrast, defects are more likely to occur during the deposition process. Since the energy difference between the ground and excited states is small, QCA devices are susceptible to transient faults induced by thermodynamic, radiation, and other impact.

The following is how a reversible logic structure differs from a traditional Boolean logic structure:

1) Requirement of equal inputs and outputs
2) Fan-out isn't allowed in reversible circuits.
3) Low number of garbage outputs leads to better and smooth architecture.
4) Reversibility must be kept strictly to a minimum level.
5) Feedbacks are not encouraged.

The following characteristics should be present in a logic synthesis technique that uses a reversible gate:

1) minimum number of garbage outputs
2) minimum input constant
3) minimum circuit level
4) minimum number of gates.

A microprocessor is a processor that combines data processing logic and control on a single integrated circuit (IC) or a small number of ICs. Combinational and sequential digital logic are also present in microprocessors. Microprocessors use the binary number scheme to represent numbers and symbols. Small computation devices were designed with loads which consist of circuit platform containing many Medium and Small scale integrated circuits, generally of the TTL kind. Microprocessors fused this into one or a few large-scale integrated circuits (IC).

A Intel 4004 microprocessor was the first to be made available.Integrating an entire CPU into a one or moreICs through Very Large Scale Integration (V-L-S-I) significantly decreased the cost of computing performance.Metal Oxide Semiconductor (MOS) design performance deliver a significant number of integrated circuit processors at a low unit price.Since there are fewer electrical contacts that can malfunction with single-chip processors, stability improves.

The project's fundamental gates are needed.

- AND Gate- The AND gate is a straightforward digital logic gate that performs logical conjunction; it operates in line with the truth table to the right. The AND gate only produces a HIGH output if all of its inputs are HIGH (1). The performance is LOW if none of the AND gate's inputs are HIGH.The function can take any number of inputs.

- XOR Gate- The XOR gate (also known as EOR or EXOR and pronounced Exclusive OR) generates a true (1 or HIGH) output when the number of true inputs is odd. An XOR gate implements an exclusive or, which means that if only one of the gate's inputs is valid, a true

output is generated. When all two inputs are zero (0/LOW) or both are one , a zero output is made.

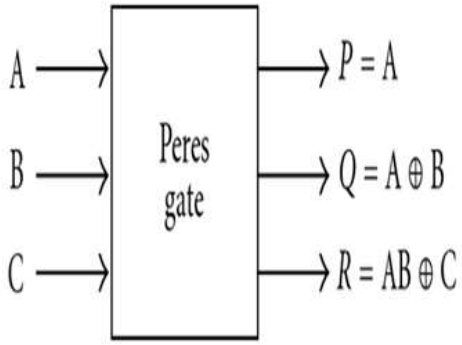
This proposed design can be further implemented in various processors for optimumperformance. This paper proposes the design of multiplier circuit with least transistor requirement made by adder taking only reversible gates.

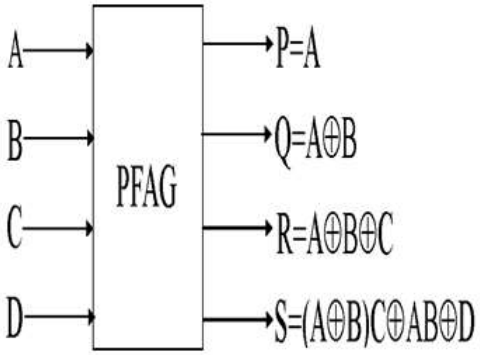
II. OBJECTIVE OF THE PAPER

A multiplier using the full adder circuit made of reversible logic for optimum performance of the processor is proposed. This concentrates on the transistor count reduction for improving the performance. This system includes both individual designs of full adder circuit using conventional gates and full adder circuits using reversible[4].

A multiplier using the full adder circuit made of reversible logic for optimum performance of the processor is proposed. This concentrates on the transistor count reduction for improving the performance. This system includes both individual designs of full adder circuit using conventional gates and full adder circuits using reversible logic gates. Finally, these individually designed full adder are cascaded to form the required multiplier circuit and the overall performance is obtained. In the proposed model, we employ the implementation of PERES Gate and PFAG gate. PERES Gate (PG) is designed of two EXOR gate and one AND gatealso . PFAG Gate is composed of 2 NOT Gates, 2 AND Gates, 4 EXOR gates. These gates are employed considering the hardware complexity. Hence, with the reversible logic we are developing a logical circuit to reduce the transistor count.

In recent years, reversible gate is emerged as the most exciting research motivation in low-power loss circuit model, with applications in low-power CMOS[13], cryptography, optical data processing, and nanotechnology.





III. BASIC TERMS USED

Reversible logic gate:

This advises us mainly for the eradication of results against input and also to balance the input from the result.

Garbage Output:

Refers to the presentation of outcomes that aren't used in the development of a given operation.These inclines are needed to achieve reversibility in assertive covering.

Constant input value}+ Input value = Garbage value + Output value

Quantum Cost:

To perform design observance results are constant, the quantum cost of the build is lower than the 2*2 integrated gates.

Flexibility:

It denotes collectivity of reversible logic gates that perform a variety of tasks.

Gate level:

This subordination towards the fraction of goals in the design which is meaningful to obtain the provided connection.

IV. IMPLEMENTATION

Themodel which comprises of different modules is primarily stationed at the origin of the desired area intended to be used. The following techniques are adapted to demonstrate the basic idea of this project:

1.Creation of full adder using conventional gates

A conventional full adder requires a total of 38 transistors, and 3 AND gates, 2 OR gates and 3 EXOR gates are used to develop a conventional full adder. This performance can further be developed by using reversible logic[7].

2.Creation of full adder using PERES gate

In several computational units, the full adder is the fundamental building block. Compatible reversible adder implementations are needed for the anticipated paradigm shift logic that is compatible with optical and quantum technologies. The performance of a complete adder circuit can be calculated using the following equations:

Sum=A⊕B⊕Cin

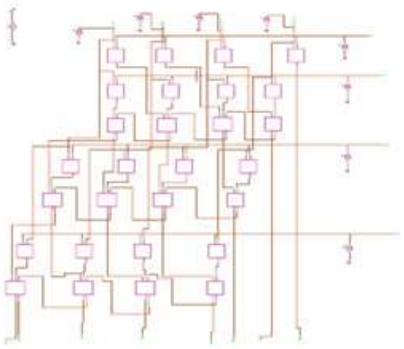
Cout= (A⊕B)Cin⊕AB

Atleast a constant input and two garbage output are used in any reversible logic realisation of a complete adder circuit.

PFAG GATE:

A full adder by PERES gate requires a total of 36 transistors, and 2 AND gates and 5 EXOR gates are used to develop a conventional full adder. This performance can further be developed by using PFAG logic.

In almost every arithmetic logic circuit, the full adder is the fundamental building block.When the gate's fourth input is set to 1, it can act as a reversible complete adder circuit on its own. (D=0)This gate's hardware complexity is lower than that of current reversible complete adder gates. This gate's quantum realisation cost is just 8. Because of its quantum implementation in NMR technology, this gate is readily available for use in nanotechnology.



3.Creation of full adder using PFAG gate

A full adder by PFAG gate requires a total of 32 transistors, and 2 AND gates and 5 EXOR gates are used to develop a conventional full adder. This is basically the advanced version of PERES gate. The PERES Full Adder Gate (PFAG) is a novel reversible full adder gate that is

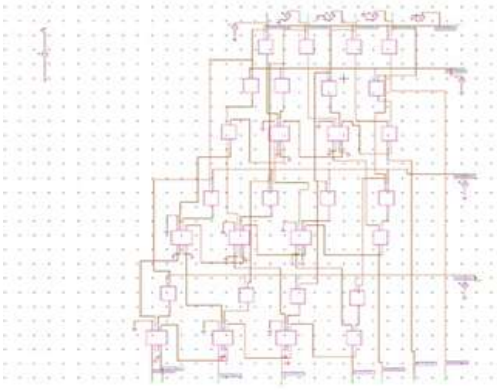
shown in figure 7. Two 3*3 PERES gates are cascaded to create the opening. Since it contains two 3*3 PERES gates, the quantum realization cost of this gate is 8.

4. Creation of multiplier circuit using conventional full adder

Multipliers are used in a variety of applications, including optical signal processing. The designed conventional full adder is then cascaded together to form the multiplier circuit, which consists of 8 full adder, 4 half adder and 16 AND gates.

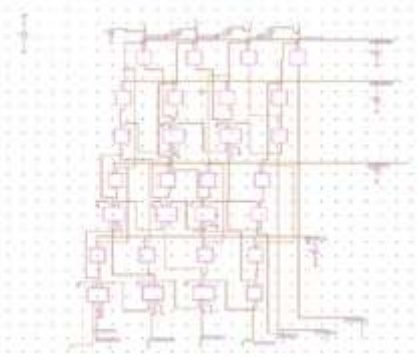
5. Creation of multiplier circuit by implementingPERESgate full adder

Designedproposed logic gate full adder is then cascaded together to form the multiplier circuit, which consists of 8 full adder, 4 half adder and 16 AND gates.Additionally , the systematic working of the respective multiplier is even more enhanced compared to the conventional multiplier, due to the use of PERES gate.



6. Creation of multiplier circuit using PFAG gate full adder

The designed PFAG gate full adder is then cascaded together to form the multiplier circuit, which consists of 8 full adder, 4 half adder and 16 AND gates. Eventhough the number of adders are similar to the previous circuit , the built design ensures that the transistor count gets reduced.



III.TRANSISTOR COUNT OUTPUT

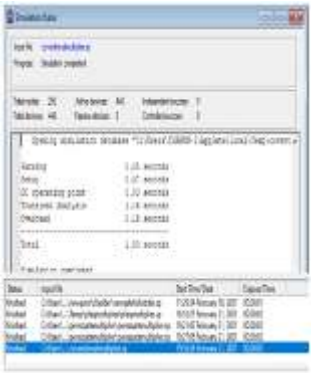


Fig 1:Transistor count output for conventional multiplier circuit

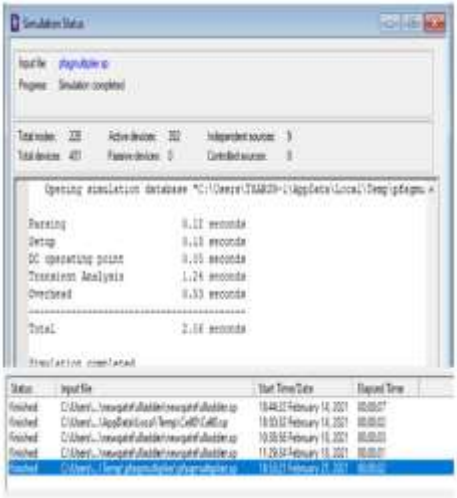


Fig 2: Transistor count output for PERES gate multiplier circuit

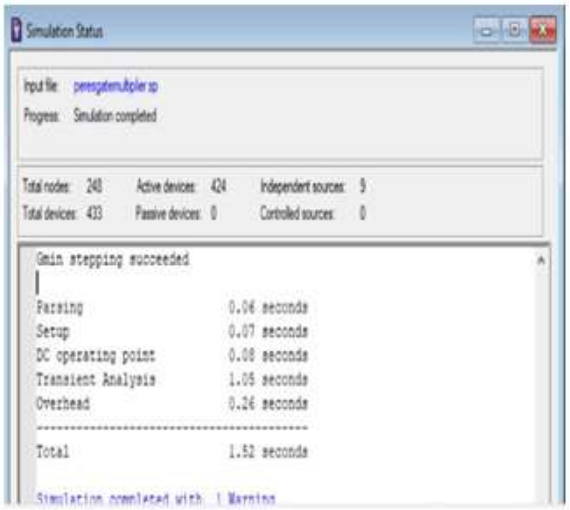


Fig 3:Transistor count output for PFAG multiplier circuit

V. RESULTS AND DISCUSSSION

The following shows that in terms of hardware complexity, quantum costs, garbage outputs, and constant inputs, the proposed reversible complete adder gate outperforms its predecessors.

Hardware Complexity: In terms of hardware contribution, this proves that this proposed reversible PFAG gate outperforms its predecessors.

Quantum Costs: The precise cost of a reversible gate is determined by the quantum logic realisation. The proposed reversible complete adder gate has a quantum realisation cost of just 8.

Our proposed model helps to reduce the transistor countby implementing a multiplier circuit using PFAG gate that reduces the transistor count drastically from 440 to 392.

VI. CONCLUSION

In nano-technology, the prescribed proposal introduces new cost efficientquantum reversible complete adder circuit. This gate's hardware complexity is lower than that of current reversible complete adder gates. This gate's quantum realisation cost is just 8. Because of its quantum implementation in NMR technology, this gate is pre - available to be used in nanotechnology.

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